Developing a low temperature Coulomb Blockade Thermometer

A Senior Honors Thesis
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by

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Abstract

We are working to develop a Coulomb Blockade Thermometer (CBT) that operates from 1K down to 30mK. While the secondary thermometers usually used can lose calibration, a CBT is a primary thermometer and would be useful for getting accurate temperature measurements. CBTs are composed of arrays of tunnel junctions designed so that the charging energy is less than the thermal energy of the electrons. The temperature can be determined by analyzing the array's conductance as a function of the voltage placed across it. We succeeded in building a CBT and performed measurements with it using lock-in techniques. However, a high junction failure rate has hampered our efforts, and it will have to be solved before we can use the CBTs effectively.

Acknowledgments

This project has proved to be a great learning experience – I have gained many skills that will surely be useful in graduate school. Undoubtedly, the most important of them is patience! In the process, I was able to work with a great group, and I owe them much for their help.

First, I must thank Dr. Rimberg. Due to circumstances beyond my control, I had to switch research groups at the beginning of the school year. Despite this short time scale for working on a thesis, he let me in to his group and guided me on this project.

Tim Gilheart was my main contact during most of this project, and he personally taught me most of the skills I needed. I am very gratefully that he spared so much of his time to help me. Otherwise, I would not have been able to learn all the fabrication steps in such a short amount of time.

The other members of the group were also a great help to me. Feng Pan guided me through the low temperature measurements, Joel Stettenheim did battle with the wire bonder to make it work, everyone was always willing to answer a quick question, and they all put up with my use (and abuse) of the lab's instruments.

I also owe a great debt to Greg Harkay who got this project started in the summer of 2006. Without the progress he made and his well kept notebook, I wouldn't have stood a chance against this project.

Finally, I'd like to thank my parents, who – while not directly involved in the project – were always inquisitive as to its status, and would listen to my rants about malfunctioning electron microscopes and the likes.

1 Introduction

There are two types of thermometers. Primary thermometers measure temperature directly, relying only on fundamental constants to convert a measured parameter in to temperature. In contrast, the measured parameter of secondary thermometers also depends on the dimensions of the thermometer, and they must be calibrated against primary thermometers. The former are generally more accurate, but are expensive, slow, and somewhat cumbersome to use. In contrast, the latter are often small and cheap, but can lose calibration over time, especially at extreme temperatures. Coulomb Blockade Thermometers (CBTs) are a relatively new type of primary thermometer developed by Pekola et al. [9] They have few of the disadvantages common to other primary thermometers – they are small, cheaply manufactured, and relatively easy to use. In addition magnetic fields have little effect on CBTs – which is not true of many other primary thermometers. These properties would make CBTs useful tools to have in our lab – they could even be added to chips containing other devices so that their temperature could be accurately monitored.

A CBT is composed of a series of tunnel junctions. These tunnel junctions are made of two metal islands separated by an insulator. Classical physics predicts that no current could flow between the islands because of the potential barrier due to the insulator, but quantum mechanics allows the electrons to tunnel through. To first order, the current through the junction is proportional to the bias voltage placed across it – it will act like a normal resistor.

However, there is a second order effect that shows up at small bias voltages. The metal islands form capacitors with the insulator as a dielectric. Thus, each electron that tunnels across the barrier charges the capacitor with energy $E_c = \frac{1}{2}CV^2 = \frac{e^2}{2C}$, so it needs a compa-

rable amount of energy before tunneling. This energy can be provided by the bias voltage as long as it is larger than $V = \frac{e}{C}$. If the bias voltage drops below this, fewer electrons will have the energy to tunnel across. Furthermore, each electron that does tunnel across increases the potential of the island, deterring other electrons from tunneling, and thus causing the electrons to tunnel one at a time – this effect is called the Coulomb blockade of tunneling. [1] The result is a drop in the conductance at low bias voltages.

If the charging energy of the junction ($E_c = \frac{1}{2}CV^2 = \frac{e^2}{2C}$) is much larger than the thermal energy of the electrons (k_BT) then the coulomb blockade is relatively unaffected by temperature. However, in the other extreme, the temperature will noticeably change the degree of the coulomb blockade.

2 Theory

I will not provide a full derivation of the theory here, but instead present the key points. A derivation for a two junction device is available in Pekola. [9]

There are two important assumptions for these results. The first is that the charging energy is much less than the thermal energy – this allows a taylor expansion in terms of $\frac{e^2}{2C}/k_bT$ – the charging energy divided by the thermal energy. Thus, the temperature range we want to measure determines how much capacitance we need – since we want the CBT to work down to 30mK, that means a relatively large capacitance and thus a large junction.

The second assumption is that the resistance of each junction (R_j) is greater than or of equal order to the resistance quantum ($R_q = h/e^2 \approx 25.8k\Omega$) – this puts us in the "weak tunneling" regime. If the resistance gets out of this range, single electron effects get swamped

out because the potential barrier is not large enough to suppress quantum fluctuations – this is the "itermediate" or "strong" tunneling regime. [1] It is possible to make a CBT with $R_j < R_q$ but corrections to the below formulas must be added, and lower resistances can lead to heating problems. [5] The weak tunneling assumption is needed to derive the electron tunneling rate: [1, 9]

$$\Gamma = \frac{1}{e^2 R_j} \frac{\Delta F}{1 - e^{-\Delta F / k_B T}}$$

Where ΔF is the difference in the electron's energy before and after tunneling. This formula can be used to find the tunneling rate in both directions across the junction, and is used to derive the below results through some clever use of steady state conditions, conservation of charge, and the assumption that electrons will tunnel one at a time and only through one junction at once.

The first important result is an equation for normalized conductance (the conductance (G) divided by the conductance at high voltages (G_T) – which is nearly constant as mentioned in the introduction). To first order:

$$\frac{G}{G_T} = 1 - \frac{\frac{e^2}{C}}{k_B T} \frac{v \sinh(v) - 4 \sinh^2(v/2)}{8 \sinh^4(v/2)}$$

Where $v \equiv \frac{eV}{2k_B T}$ and V is the bias voltage. A curve of this form is shown in figure 1.

From the previous result it can be shown that:

$$\frac{eV_{1/2}}{2k_b T} = 5.439...$$

$V_{1/2}$ is the width of the conductance curve half way between the bottom and the top of

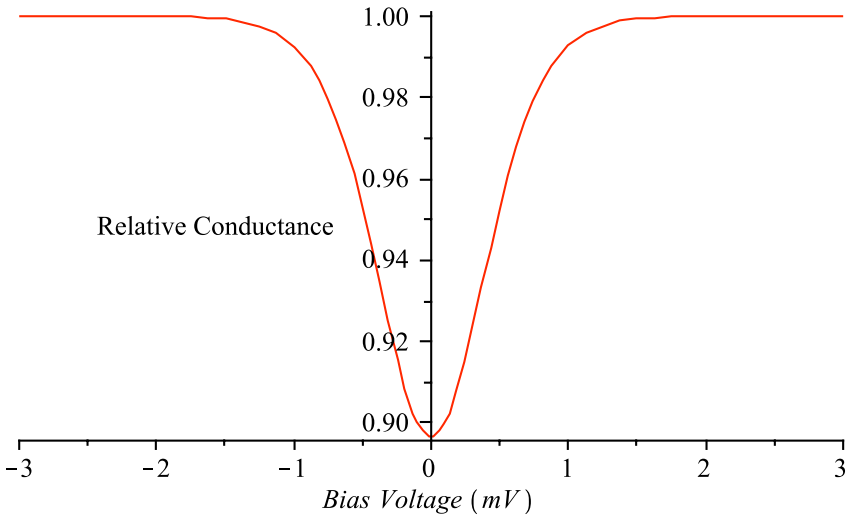

Figure 1: An example conductance curve for an array with two junctions each with 3fF capacitance at 1K.

the dip. Since the right side is a constant, this allows us to use the array as a thermometer. Since it does not depend on the CBT's dimensions (like C), it is a primary thermometer. Experiments have shown the intuitive result that the width of the dip scales linearly with half the number of junctions. Making a CBT with many junctions is useful because it increases $V_{1/2}$ at lower temperatures, leading to better measurements. Long arrays of junctions also lessen the effects of higher order tunneling phenomena. [9]

It should be noted that there are other ways to use CBTs. For example, Bergsten et al. have shown that it can be done by taking the third derivative of current as a function of voltage and examining the zero crossings. With proper instrumentation, this allows the temperature to be measured quickly. [3] However, we used the previous method.

3 Fabrication

3.1 Overview

Fabrication is the difficult part of this venture. The process takes many steps and has many parameters to tune, so there are many places to make mistakes. Parameters are tuned primarily through systematic trial and error (e.g. find a value that's too high, then one that's too low, and then searching in between).

The basic steps are design, sample preparation, electron beam lithography, and evaporation. The last three steps are depicted in figure 2 and there is a subsection devoted to each.

3.2 Design

The device's layout is saved in a pattern file created with DesignCAD – a program integrated in to the Nanoscale Pattern Generation System (NPGS) software that controls the electron beam lithography system. Much of the design work was done by Greg Harkay during the summer of 2006. The dimensions of the system were chosen based on the experiments of Pekola and Bergsten in the weak tunneling regime [2, 4, 7–9] as well as our lab's experience with making tunnel junctions.

Figure 3 shows the design we have been using for testing. It consists of one array of 50 tunnel junctions with bonding pads and a grounding bar. The overall dimensions are 1000 by 400 μm. The bonding pads (yellow) are where we attach the wires to do measurements. The grounding bar keeps both ends of the array at the same potential – the junctions are static sensitive and this keeps them from getting zapped. The grounding bar is broken once

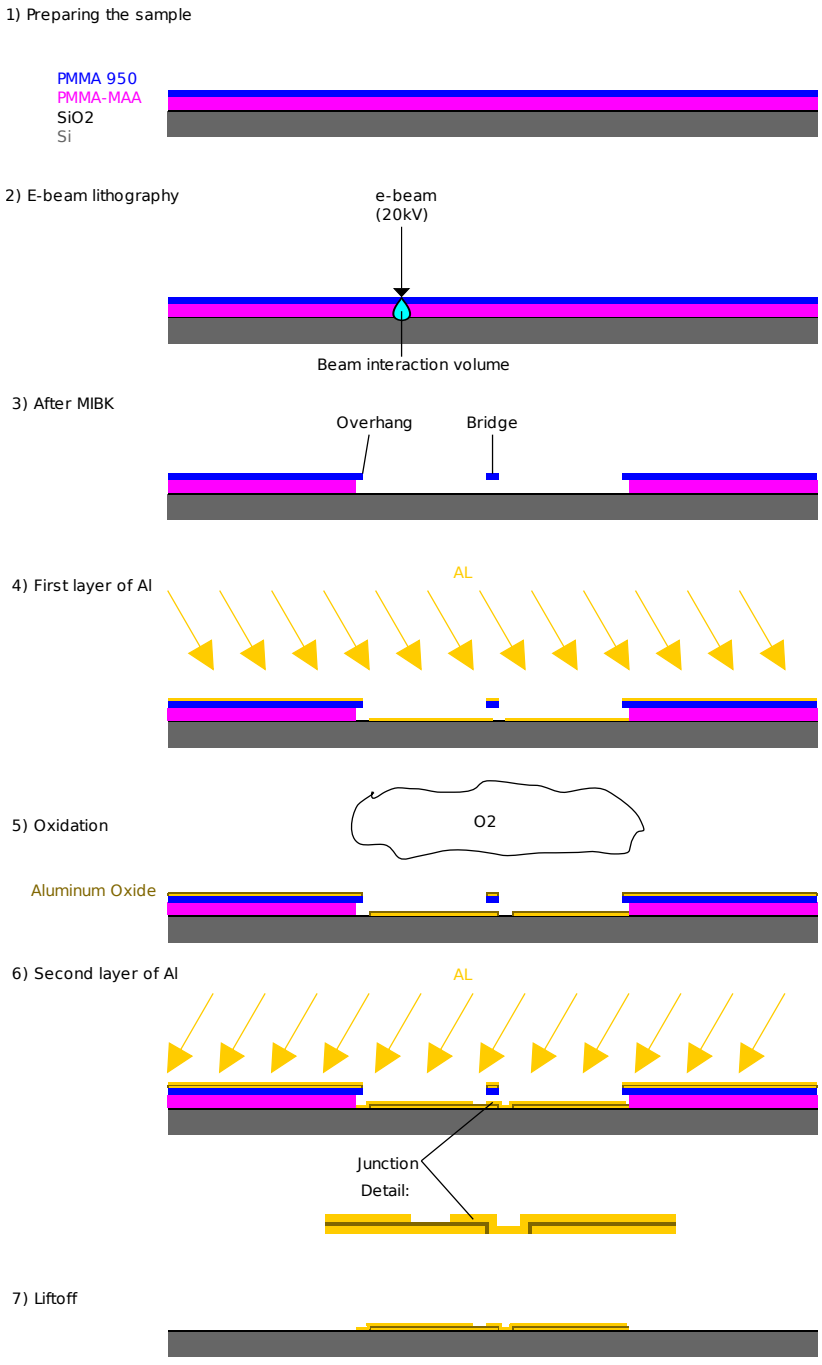

Figure 2: Basic steps to make a device.

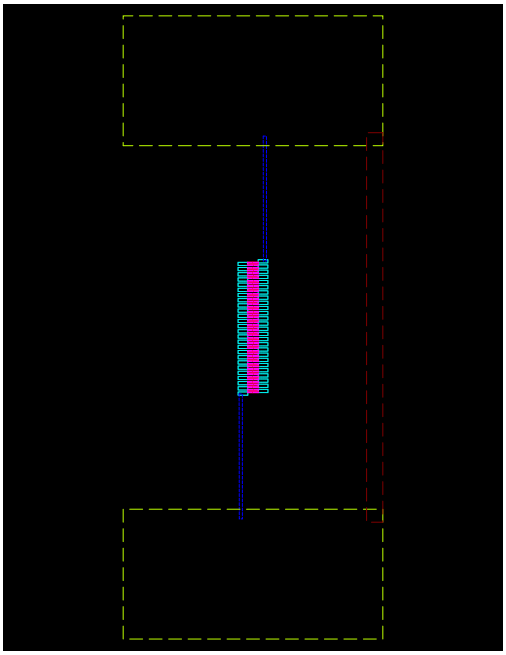

Figure 3: The device.

the device is wired up since both ends of the device can be grounded by our test fixtures. The junctions are in the middle of the magenta rectangles – they are formed by a $\approx .1\mu$m gap in the middle that isn't visible in the figure. The magenta rectangles are 1μ tall, and are drawn in two parts. First the whole area is drawn, and then the perimeter is redrawn. Doing this helps make a clean edge, which is important for creating working junctions. The light blue areas are fins – they have dimensions of 4 by 15μm. Besides connecting the junctions together, their larger area helps the device stay at the temperature of the substrate. [7, 8] Finally, the dark blue areas are the leads the connect the array to the pads.

After using DesignCAD, a different program component of NPGS is used – the run file editor. A run file holds all the information needed by the lithography system. It can contain multiple pattern files, instructions about their relative placement, and the magnification and

currents the different parts of the device(s) should be drawn with. The run file associated with the design in figure 3 draws two of the devices 700μm apart. Making individual arrays allows us to learn about the distribution of their properties (despite our best efforts, arrays made at the same time will not all come out the same). However, we have made other run files that draw the array portion multiple times with leads connecting them in parallel. This is the configuration we will use once we have finalized our design. Having several of the arrays in parallel lowers the total resistance. This makes it easier to do radio frequency (RF) measurements (our eventual goal) and adds redundancy so that the device will work even if some of the arrays are broken.

The run file editor calculates the magnification necessary to fit the parts of the device in the microscope's field of view. The pads and grounding bar are drawn at a magnification of 50x, the leads at 100x, and the fins and junctions at 400x. The CAD program allows us to assign all components at the same magnification to be in the same "layer" – they all are drawn at the same time. The alignment changes slightly whenever the microscope changes magnification, so features in different layers are drawn with some overlap so that they will still connect.

The beam current is set at this stage but is adjusted later. However, dosing issues must be taken in to account during the design. For example, to draw the large pads in a reasonable amount of time, we use a high current. However, even with a well focused beam, some of this current will ended up elsewhere, so we need to place the pads far away from the junctions, which are drawn with a smaller current for more detail. There are also proximity effects within the array – the junctions in the middle will get a higher dose than those on the end, since there is more being drawn around them. If this were to prove too much of a

problem, we could draw the junctions with different dosages depending on their positions within the array, but this did not prove necessary to get a working device. It is something worth investigation in the future because of our low CBT yield (more on that later).

3.3 Preparing the Sample

For our substrate we use silicon with a 380nm layer of silicon dioxide insulator grown on it – the substrate acts only as a place to put the device and has no part in its function. After cutting a chip, it is coated with e-beam resist. We use two types of positive resist – resist that is weakened by the electron beam. For the top layer we use polymethyl methacrylate (PMMA) – the polymer that makes up plexiglas. The variety used has an average chain weight of 950,000amu, and it comes dissolved in an solvent. When we bake it, the solvent is driven out and the polymer chains cross link.

For the bottom two layers we use a mix of PMMA and methacrylic acid (MAA). These are coplolymers which cross link during baking. However, the cross links between the different polymers are much less strong than between the same polymers. This make the copolymers much more susceptible to the electron beam – the beam's primary way of weakening the resist is by destroying the cross links, not by actually breaking the polymer chains.

The weaker resist is on the bottom so that we can get the undercut necessary to form resist bridges – the electron beam bulges out in to a tear shaped interaction volume when it hits the resist, so it affects a larger volume of the bottom layer, but the beams energy is thus diluted (see figure 2). Two layers of the weaker resist are applied to increase the height of the bridge.

The step by step process is:

1. Cut the chip – be careful not to scratch it.

2. Sonicate the chip in acetone for 10 minutes – insufficient cleaning will cause the resist to coat the chip unevenly.

3. Heat one hot plate to 90C and another to 150C.

4. Rinse the chip with isopropanol (IPA) and blow dry with nitrogen.

5. Clean three plastic pipets by blowing with nitrogen.

6. Place a brass plate on the spin coater, apply several drops of PMMA 950 with one of the pipets (it will act like glue), and spin at 1000rpm for 10 seconds.

7. Affix the chip to the plate, and bake for 5 minutes at 90C.

8. Spin 1 drop of PMMA-MAA on to the chip at 3000rpm for 30 seconds then bake for 10 minutes.

9. Repeat the previous step once.

10. Spin 1 drop of PMMA 950 on to the chip at 3000rpm for 30 seconds and then bake for 10 minutes.

11. Place 2 small marks of silver paint in opposite corners – this is used for focusing.

3.4 Electron Beam Lithography

The electron beam lithography is preformed on a scanning electron microscope in Dartmouth's Rippel Electron Microscope Facility (FEI company's model XL-30 ESEM-FEG)

that is controllable by the NPGS software and hardware. The NPGS hardware consists of several digital to analog converts which can direct the motion of the electron beam and control a fast beam blanker, so that the beam can be blocked while being moved.

The NPGS software automates most of the lithography – all that the user has to do is change magnifications and beam currents when prompted. However, before lithography can proceed, the microscope must be set up. The most important step is getting a good focus on the surface of the chip. The silver paint applied during sample preparation is used to get a rough focus – the chip itself is so smooth that there are often few features to focus on. However, this focus is not good enough for our purposes. To get a better focus, we burn a hole in the resist by holding a low current beam in one spot. Then we focus on the edge of this hole at 80,000x magnification. This is done once (or more if a good focus cannot be achieved the first time) between every pair of devices – because the devices are large and spaced far apart (as far as electron beam lithography goes) and because the chip cannot be mounted perfectly level, the focus can change significantly from one spot to another. This is why the devices are drawn in pairs – initially they were drawn 8 at once, but we found that some of the devices were drawn out of focus.

Each device of the design shown in figure 3 takes about 11 minutes to draw and I usually make 8 to 10 at a time because they have a high failure rate, so this step takes a fair amount of time. These devices are at the large end of what we fabricate with electron beam lithography – once the design is finalized it might make sense to adapt it to photolithography since that would allow the devices to be made much more quickly.

As stated in the previous section, the function of the electron beam is to weaken the cross links in the resist. In the next step, the weakened resist will be removed, leaving the

unaffected resist behind

1. Mount the holder with the gold standard and the faraday cup in center hole. Mount the samples with conductive tape.
2. Vent the chamber, disconnect the grounding wire, put in the sample holder, and pump down.
3. Insert the beam blanker, turn on the blanker power supply, and start the NPGS software.
4. Turn on the accelerating voltage – 20kV.
5. Get a good focus on the gold standard at 40,000x – adjust stigmation as necessary.
6. Measure the beam current at the appropriate spot sizes. Input this data in to the run file.
7. Move to the sample and find a corner with silver paint, change to 7.5mm working distance, and get a good focus. Note the coordinates
8. Go to the opposite corner and do the same. Calculate the location of the center.
9. With the beam blanked, go to appropriate place on the sample
10. Make a focusing hole by changing to spot size 2 in spot mode, unblanking the beam, and waiting 2 minutes. Get a good focus on the hole.
11. Use the NPGS software to the draw the pattern.

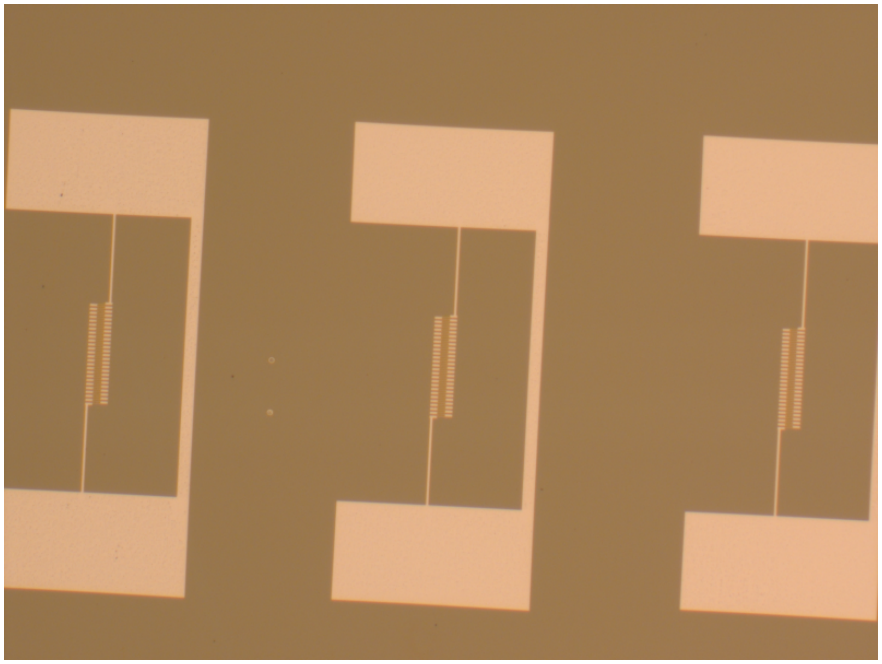

Figure 4: Several arrays after evaporation. You can see two focusing spots between the left two arrays.

3.5 Evaporation

The first step is to remove the resist that has been weakened by the electron beam (see figure 2 part 3). This is accomplished by a short rinse in methyl isobutyl ketone (MIBK), a solvent weak enough that – if used quickly – it will only remove the resist with weakened cross links. This exposes the substrate where we wish to deposit metal, and leaves resist everywhere else. Because of the difference in strength of the resists, and the spread of the beam once it encounters the resist, this is also the step where the bridge is created.

1. Dunk the sample in MIBK diluted 1 to 3 with IPA for 1 minute.

2. Clean the sample in IPA for 40 seconds

3. Blow the sample dry with nitrogen.

The next step is evaporation using the double angle technique (also known as shadow evaporation). For this, we use an evaporator in our lab. First a layer of aluminum is deposited at and angle slightly off from perpendicular while the chamber is at vacuum. Then, oxygen is let in to the chamber and a layer of aluminum oxide forms on the deposited layer. The oxygen is then pumped out and another layer of Al is deposited from the supplementary angle.

The effect of this procedure can been seen in figure 2, step 5. Over most of the chip, evaporating from different angles has no effect – it simply forms an aluminum, aluminum oxide, aluminum sandwich. However, at the junction, something else happens. If everything went as planned, there is a PMMA 950 "bridge" left there. This leaves a "shadow" – it blocks the aluminum from reaching the substrate – in different places depending on the evaporation angle. During the first evaporation, it leaves a gap in the deposited aluminum to one side – during the second evaporation it leaves a gap to the other. These gaps can be thought of as an open faced sandwich (aluminum, aluminum oxide) and just a piece of bread (aluminum) respectively. There is no continuos layer of aluminum running from one side to the other, instead current must run through the aluminum oxide – in the region between the two gaps – in order to make it from one layer to the other and thus to reach the other side. The amount we tilt the sample determines the distance between the gaps, and thus affects the the capacitance and resistance of the junction.

The difficult parameter to tune during this step is the amount of oxidation. It can be controlled in two ways – changing the amount of oxygen let in to the chamber, and changing how long it remains there before being pumped out. This has proved to be the most difficult

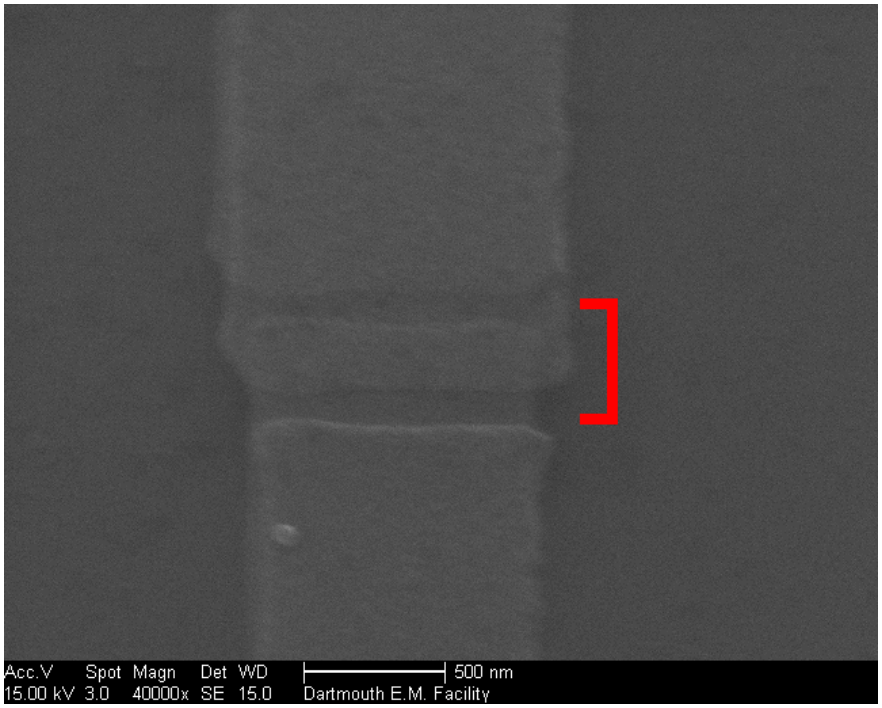

Figure 5: Image of a well formed junction (extents shown in red) after evaporation (picture taken with the SEM). Unfortunately, the 15kV electrons in the beam break the oxide and destroy the junction, so it cannot be used after imaging

parameter to tune – in part because the function of junction resistance vs oxygen is highly non-linear – resistance increases exponentially with oxide thickness, and the oxide thickness increases in a very non-linear fashion over time. For this reason, I have spent most of my time trying to tune this parameter.

The final step is to remove the remaining resist and the aluminum that has formed a film on top of it – this step is called "lift off" (see figure 2 part 7). To do this, we just set the sample in acetone – a strong solvent that dissolves all the remaining resist.

1. Load the sample and aluminum in the evaporator.

2. Pump down to $\approx 10^{-6}$torr.

3. Tilt sample up 8 turns.

4. Evaporate from source A – deposit $165\mathring{A}$ at $3-4\mathring{A}$ per second.

5. Close gate vale and let in oxygen in the form of 95% Argon 5% oxygen gas.

6. Wait.

7. Pump back down to $\approx 10^{-6}$torr.

8. Tilt sample down 8 + 8 turns.

9. Evaporate from source B – deposit $260\mathring{A}$ at $4-5\mathring{A}$ per second.

4 Testing and Results

4.1 Room Temperature

Although the thermometers do not function at room temperature, we first test them at room temperature to determine the resistance of each array. We are aiming for $R_j \approx R_q$ since larger resistances are undesirable for measurement purposes, and smaller resistances lead to unwanted tunneling effects. Since our arrays have 50 junctions, that means we want a resistance of $\approx 1M\Omega$.

To perform these measurements we use a standard four probe setup with two lock-in amplifiers – one measures the voltage across the CBT and the other one measures the current through it. Together, these tell us the resistance. The input signal is a 100μV 11Hz sine

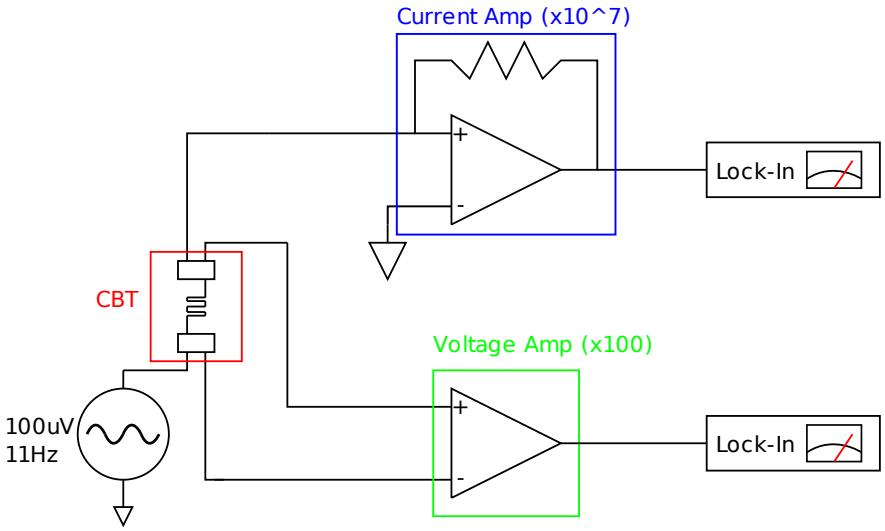

Figure 6: The room temperature measurement setup.

wave created by one of the amplifiers and synced to by the other. The lock in amplifiers allow us to use a small bias voltage while still taking low noise measurements. See figure 6.

These measurements were used primarily to tune the oxidation parameters. I started with the recipe our lab uses for making single electron transistors – which have two tunnel junction that are much smaller than those in the CBTs. These parameters proved to be much to low for the CBT's large junctions, and our low CBT yield made it difficult to tune the oxidation – we were mislead more than once by dead junctions.

The testing procedure is as follows:

1. Glue the chip to the sample holder with rubber cement, and use the wire bonder to connect the devices to the sample holder's pads.

2. Measure the resistance of each device – since the grounding bars are still in place, the resistance should be very small. If this is not the case, rewire the bad connections.

3. Now, break all the grounding bars by scratching through them with a pointy object. Make sure the sample holder's removable grounding bar is attached to provide static protection.

4. Measure the devices again – this time we see the actual resistance of the array

Each array can come out in one of four ways: it can fail open (very high resistance), fail closed (very low resistance), have an intermediate resistance, or have been bungled during fabrication (e.g. I forgot to change magnification when switching layers, or I scratched the array while trying to break the grounding bar). Open failure is very common since only one part of the device has to fail (the chain is only as strong as the weakest link). Assuming that these failures occur randomly in an uncorrelated fashion, some back of the envelope calculations shows that each junction (or leads to the junction) has a $\approx 2\%$ probability of failing in this way. Our choice of 50 junction long arrays was fairly ambitious (many CBT are made with fewer) and we pay the price in our high failure rate – making shorter arrays would boost the yield significantly.

Failing closed is less likely because all of the junctions need to fail closed – it indicates something went very wrong during fabrication. Finally, even if the array does not fail in one of those ways, it still needs to have the right resistance. Since we want $R_j \approx R_q$, and we assume that some junctions will fail closed even within working arrays, that means we are shooting for around $1M\Omega$. Failing due to user error has (thankfully) become less common as I gained experience – a good thing since it is the most easily prevented type of error!

The resistance is tuned by controlling the oxidation. The results are shown in Table 1.

Date Made	Pressure (mTorr)	Time (min)	Design	Failed user	Failed Open	Failed Closed	Resistances (kΩ) & Notes
2/28	?	?	9 in parallel	?	?	?	380, Tested 3/26
4/8	120	3	9 in parallel	≥1	?	?	Short, Tested 4/15 left in MIBK too long, arrays damaged
4/28	120	3	6 separate	2	0	0	21, 22, 55 one killed by scope problem
4/29	1000	4	7 separate	1	0	6	possible focusing problem
4/30	1000	4	8 separate	3	5	0	Initially took 25M resistance measurement at face value
5/1	500	4	8 separate	4	4	0	Also initially took results at face value
5/5	300	4	8 separate	4	0	0	30, 24, 30, 24, tested 5/6
5/8	650	4	8 separate	1	0	0	23, 40, 29, 34 only tested one of each pair
5/9	1300	4	8 separate	5	1	0	234, 10000, second may be a short
5/13	1300	7	6 separate	0	6	0	
5/14	1375	6	6 separate	0	2	0	microscope problem caused bad litho
5/16	1400	6	4 separate	1	3	0	
5/16	1300	5	6 separate	1	3	0	55, 102
5/19	1300	6	6 separate	1	3	1	714
5/20	1300	6	6 separate	0	3	1	230, 80
5/20	1300	6	4 separate	0	1	0	40, drawn with higher current 2 not tested due to space constraints

Table 1: Information for all arrays that we measured. Unknown quantities are designated with question marks. "Pressure" and "Time" are for the oxidation procedure described earlier. If a device was not measured the same day it was made, it is noted.

A number of arrays were made but were never test because they were obviously damaged. Several of these failures were caused by microscope problems – the stage, computer, and x-ray detector were replaced early in the spring term. Only the first two directly hindered lithography, but maintenance of all three took the microscope out of service for over a week in total.

It is difficult to interpret the results in table 1 without some context. We started by making many array wired in parallel, but we decided that it would be best to make individual arrays so that we could learn about the distribution of their resistances. After learning that 120mTorr was not enough pressure for our desired resistance, we tried to find an upper value so that we could bracket our search. We thought we had accomplished this after measuring our 1torr devices, but after trying lower pressures, it became clear that 1torr was not an upper bracket, and our devices had simply failed. This was in line with the first device in the table, which I accidentally exposed to ≈10torr for a short time (it had also spent several

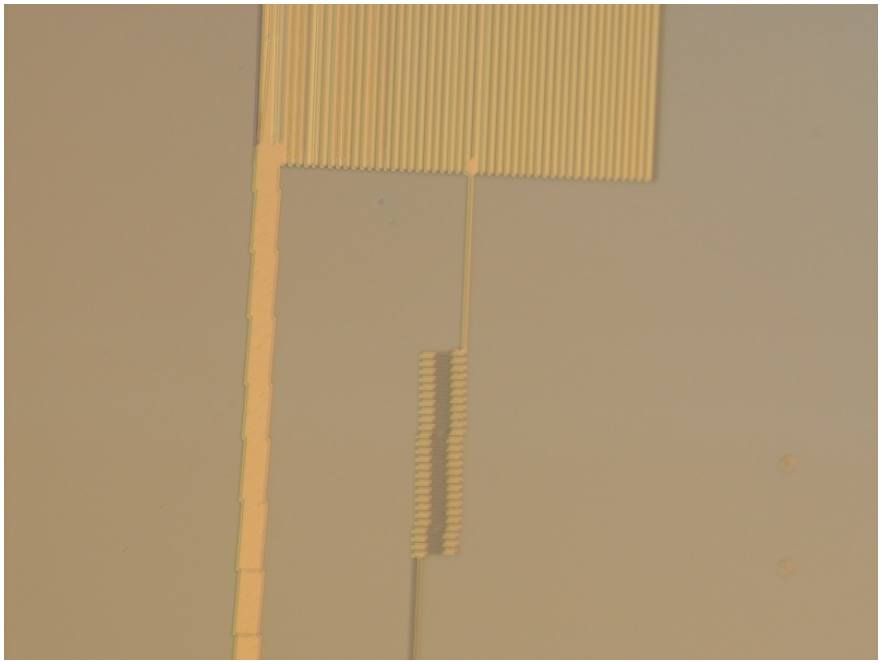

Figure 7: An example of how the electron microscope can ruin a device (and your day). This was caused by a stage problem.

weeks sitting at atmosphere, resulting in additional oxidation).

After realizing that we were not getting a thick enough oxide layer, we upped the pressure and time. However, after a certain point, increasing the pressure resulted in complications (more work to pump out) so we increased the duration instead. Several promising devices (5/9, 5/19, and 5/20) have lead us to believe that we are now in the right ballpark. However, our low yield makes it hard to tell. We attempted to measure those three devices at low temperatures – see the next section.

The cause for our low yield is not entirely clear – however there are several possibilities. Our evaporation chamber may been exposed to pump oil from our diffusion pump. A common symptom of this is that many devices have very low or very high resistances but few have intermediate resistances. However, other group members used the evaporator without much issue, so this is not our leading hypothesis.

A more likely explanation is that I have been using too low currents during lithography – the edges of the metal in the devices are often somewhat ripped up (see figure 7). Sometimes it is even possible to spot a tear all the way through the metal (causing an open failure), but often it is not. However, a few recent experiments with fabricating shorter arrays (5 junctions instead of 50 – leading to lower dosages due to proximity effects) and drawing the large arrays with more current seem to point in the opposite direction – that our dosages are too high. The short arrays came out with less jagged edges and the higher dosed arrays also had jagged edges. This may be because, in some regimes, the PMMA-MAA resist can act as a negative resist – higher current strengthens it.

A final possible cause, or at least confusing factor, is the age of the resist. Resist is finicky stuff – slight changes in the resist (such as exposure to ultraviolet) can lead to large

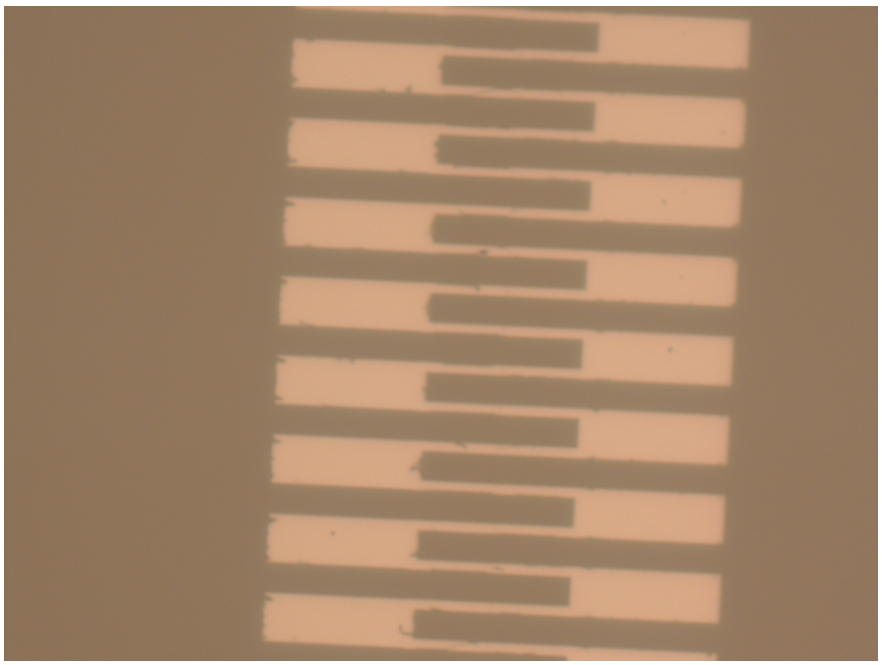

Figure 8: This array shows rips and torn up edges – however it is not as bad as for many arrays. (Optical microscope at 100x)

changes in lithography. I have my own vials for storing resist so that the large bottles are not exposed to light and atmosphere every time I need to prepare a sample. In early May, I used up all the resist in my vials so I refilled them. Even though I refilled the vials from the same batch of resist that they initially held, this could have affected the lithography – perhaps driving the yield down at a time where it should have been going up due to my increasing experience and fine tuning of procedures. Around the time I refilled my vials, the size of the focusing holes I burned increased markedly. This could be evidence that the new resist had affected the lithography. However, this was also right after the microscope was serviced and the beams re-calibrated – another possible explanation for the larger focusing holes.

In short, we have no conclusive answer for why our yield is so low. However, there is no reason to believe that, given enough time, the yield could not be improved through addressing these and other possible issues.

4.2 Low temperature

In order to test a CBT, we need to measure it at low temperatures. There are several challenges to doing this. The first is that devices need to be moved to our lab's Oxford Heliox AC-V ^{3}He refrigerator which is a non-trival task because the devices have to be disconnected from the room temperature sample holder and rewired to a different sample holder that fits in the fridge. Because the grounding bars have been broken for room temperature testing, this makes the devices very vulnerable to getting zapped. This is what happened to the sample from 5/19 and may have also been the fate of the device from 5/9. To solve this problem, we wired the devices from 5/20 directly to the low temperature sample holder so

that it was not necessary to rewire them.

Another issue is that aluminum becomes super-conducting at 1.2K, and we need to prevent that from happening. In order to do so, we placed a strong permanent magnet near the device. Depending on the orientation, a field of .05-.2T might be necessary [7] – the magnet we used has a maximum strength of $\approx .2T$ nearby and got the job done.

I will not relate the steps necessary to work the refrigerator – even though it is fairly simple to use (by low temperature refrigerator standards) there are many steps and it would not be beneficial to list them. The theory is fairly straight forward – a pulse tube cryocooler cools a ^{3}He reservoir to around 3K. Then, the ^{3}He is allowed to cool the sample to $\approx .3K$ evaporatively. This is a one shot process – after the ^{3}He evaporates it must be recooled to repeat the process. However, it can keep a sample at $\approx .3K$ for almost two days, which is more than enough time to perform our measurements. The whole cooling process takes about 2 days.

Our low temperature measurement setup (see figure 9) differs from the room temperature setup because we need to measure current as a function of voltage over a range of several mV. To do this, we add a ramp to sine wave from the lock-ins – this requires another amplifier. The current amplifier is used to mirror this signal to the CBT, and the buffer is used to prevent the lock-in from injecting any noise in to the current. The lock-ins only measure the small AC signal, not the DC ramp, but because the DC bias affects the CBT's resistance, the AC signal is likewise affected. Thus, conductance can be measured as before – by dividing the AC current through the device by the AC voltage across it.

In the end, we were only able to measure one working device – the 230kΩ device from 5/20. I tried to measure the devices from the same day with smaller resistances, but both

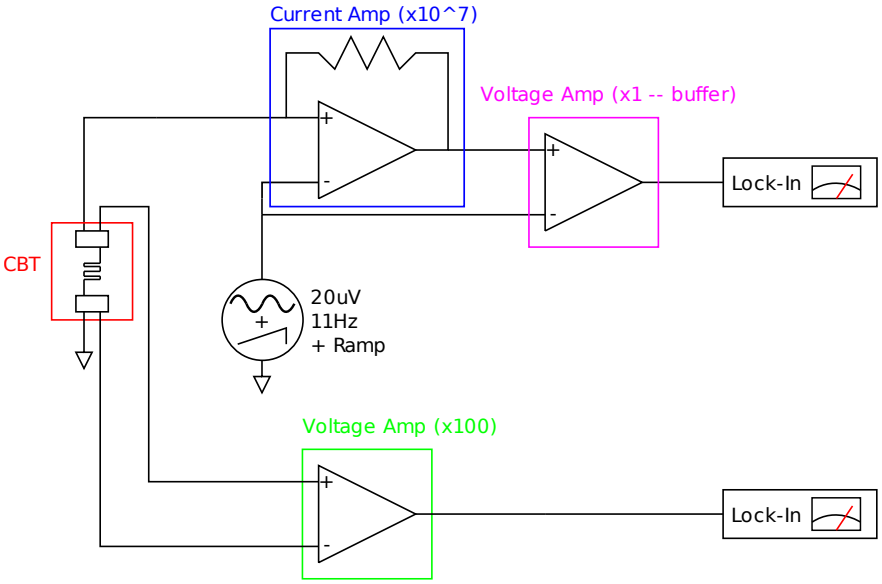

Figure 9: The low temperature measurement setup.

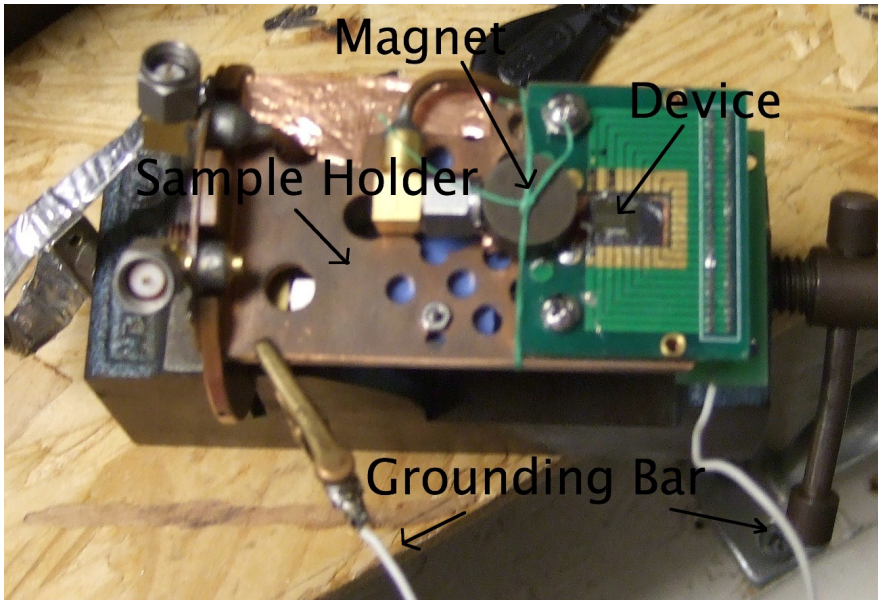

Figure 10: The sample holder used for cold measurements with the 5/20 chips attached

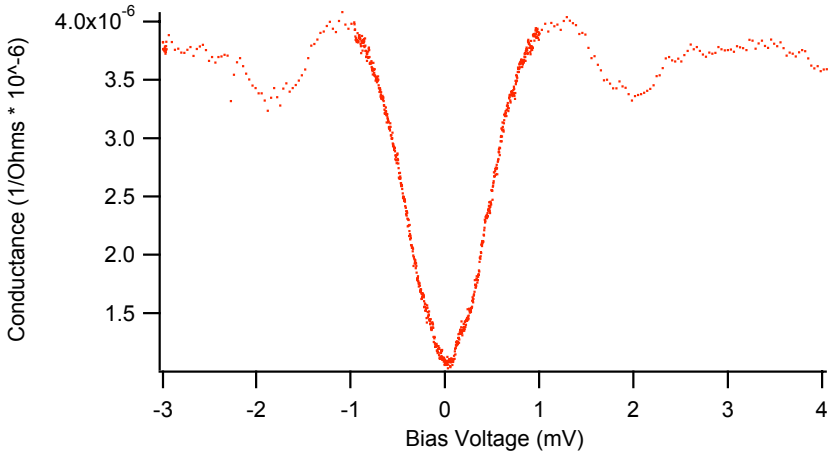

Figure 11: The conductance curve at .285K

appeared to be open circuits. I did not get a chance to retest them at room temperature, but I assume they must have been damaged somehow. The working device was tested at two temperatures – .285K and 2.262-2.288K (the latter temperature was done while the fridge was warming back up, so it covered a range of temperatures) – we would liked to have tried other temperatures but we did not have time. The conductance curves can be seen in figures 11 and 12.

The center section of the .285K curve and the whole of the other curve were done with a bias voltage ramp of $\approx 3\mu$V per second. The extremities of the .285K measurement were done with a faster ramp. The conductance dip around zero bias voltage is clearly visible in both measurements, although the signal to noise ratio is obviously much lower in the higher temperature measurement. This is not too surprising – the CBTs were designed for use under 1K.

We have not performed a careful analysis of this data because this device is not operating in the weak tunneling regime – $R_j < R_q$. If all the junctions are working then $R_q \approx 5k\Omega$.

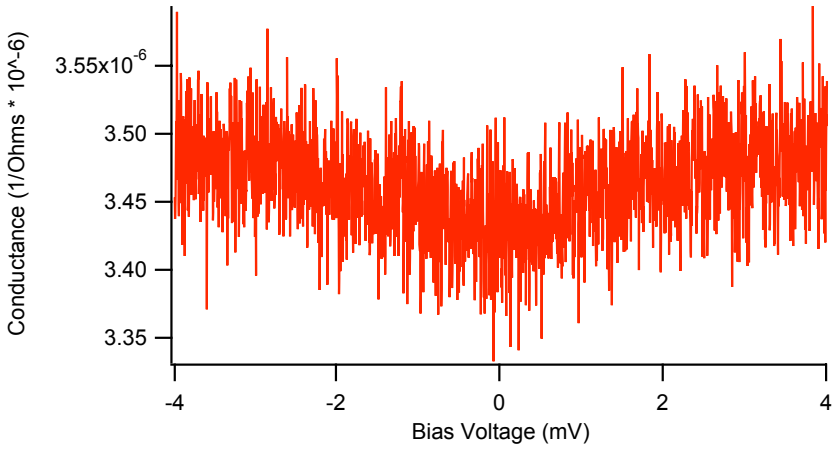

Figure 12: The conductance curve at 2.262-2.288K. Lines have been drawn between the points for added clarity

The number of working junctions could be measured by allowing the device to superconduct and measuring the superconducting gap – it should be 4 times the number of junctions times the known superconducting gap of aluminum.

It is simple to see that the weak tunneling regime formulas fail – estimating $V_{1/2} \approx 1mV$ we get a temperature of $\approx 1K$ using the two junction model. This temperature is around 4 times the measured temperature, and that's not even including the effects from having multiple junctions. It is also likely that the device has inhomogeneous junctions – applying some of the rough corrections from the non-weak tunneling regime [4] brings us closer to the measured temperature, but still not close enough.

The small dips to both sides of the central valley are somewhat unexpected, but remained on subsequent re-measurements, so it is safe to assume that they are real. It likely indicates that the junctions are not homogeneous, which unsurprising since a device with a resistance of 80kΩ was made in the same batch.

5 Conclusion

Although we have not created a fully usable CBT, we are getting tantalizingly close and we have produced a CBT which is almost there. A high failure rate hindered our progress – our fabrication procedures obviously require fine tuning to finish of the task, but our parameters appear to be largely correct. In my estimation, it it the lithography dosages that need the most work – it is possible that some small changes could dramatically up the yield. Another possible solution lies in changing the bottom resist. Most of our group has abandoned the PMMA-MAA copolymer in favor of PMMA 450, which is the same as PMMA 950 except it has an average chain length less than half as long – this makes the resist weaker since it has less opportunities to cross-link. This could avoid negative resist effects.

Further work also needs to be done in characterizing the junctions. During our low temperature measurements, we recorded the phase as well as the magnitude of the signal – this might allow us back out some information about C. It may also be possible to learn about the capacitance by measuring the depth of the normalized conductance dip as a function of temperature. [4] Allowing the aluminum to superconduct and measuring the superconducting band gap would allow us to learn more about the closed failure rate of the junctions.

Finally, the CBTs need to be tested at more temperatures to make sure they work across the intended range. This can be done using our lab's dilution refrigerator and we could use known physical effects for temperature comparison (e.g. Ti superconducts at .4K).

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