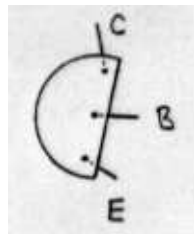


EXPERIMENT 9: BIPOLAR AND FIELD EFFECT TRANSISTOR CHARACTERISTICS

In this experiment we will study the characteristics of bipolar and junction field-effect (JFET) transistors, and will learn to use the transistor curve tracer.

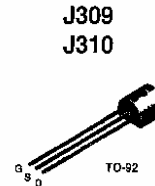
Be sure to observe the proper orientation of leads when you install the transistors in the test setup and the curve tracer.

VIEW FROM ABOVE
BIPOLAR



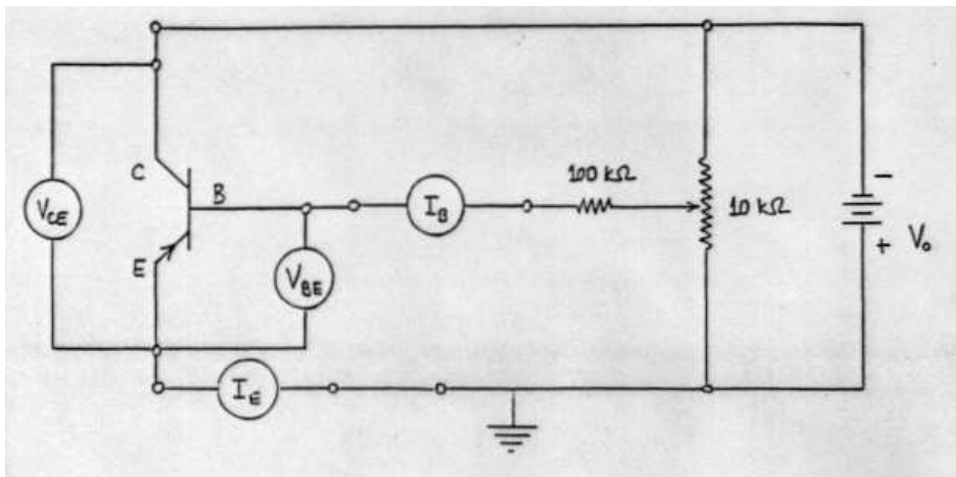
(leads point away from you)

N Channel FET



I. THE BIPOLAR TRANSISTOR

The circuit we will use to measure the properties of a silicon PNP transistor (model 2N3906) is shown below. Use a DC power supply for V_0 . For ammeter I_B use a VOM on the 0-50 μA scale; for I_E use a second VOM with the scale set to 1, 10, or 100 mA as needed. Use digital meters to measure the voltages V_{BE} and V_{CE} .



1. The first step is to measure I_E and V_{BE} as a function of the base current for a fixed value of V_{CE} . Turn the 10 k Ω pot all the way down (i.e., full counter-clockwise). Next, connect the ammeters being careful to observe the proper polarity and then connect up the power supply, again being careful to observe the polarity. Make the remaining connections, and then turn on the power supply and adjust V_0 so that $V_{CE} = -12$ V. By adjusting the pot you can change the base-to-emitter voltage, V_{BE} , and hence the base current I_B .

Measure and tabulate I_E and V_{BE} as a function of I_B taking 2 μ A steps for $0 \leq I_B \leq 10 \mu$ A and 5 μ A steps for 10μ A $\leq I_B \leq 50 \mu$ A. You will notice that V_{BE} drifts slowly for some time after I_B is increased or decreased. This drift is due to the temperature change caused by the power dissipation in the transistor. After each change in I_B you should pause briefly (≤ 1 minute) to allow the temperature to stabilize before taking the readings.

You will also notice that V_{CE} changes some (particularly when you change scales on the ammeter I_E). You may reset V_{CE} to -12 V at each step if you want, but it is also all right to just ignore the changes, since I_E and V_{BE} are nearly independent of V_{CE} .

Calculate h_{FE} (or β) at each point from the formula $\beta = I_E/I_B$ and make a graph of β as a function of I_E .

2. For signal transistors such as the one we use in this experiment, the relationship between V_{BE} and I_E (or I_C) is given approximately by:

$$I_E = I_0 \left(e^{V_{BE}/V_{KT}} - 1 \right)$$

provided that T is constant (I_0 and V_{KT} both depend on temperature). Make a graph of I_E vs V_{BE} on semilog paper, and verify that the low-current (i.e. constant temperature) portion of the graph is linear. Determine the quantity V_{KT} from the slope of the linear part of the graph, assuming that $V_{BE}/V_{KT} \gg 1$. How does your result compare with the expected value, $V_{KT} = kT/e = 26$ mV?

3. The quantities I_E and V_{BE} are approximately independent of V_{CE} . In this step we will measure two parameters, the output admittance (h_{oe}) and the reverse voltage ratio (h_{re}) that give the sensitivity of I_E and V_{BE} to changes in V_{CE} .

Adjust the power supply voltage V_0 to obtain $V_{CE} = -8$ V, and then adjust the 10 k Ω pot to get I_B 15 μ A. Record the values of I_E , I_B , V_{BE} and V_{CE} . Then adjust the power supply and the pot to get $V_{CE} = -16$ V and the same value of I_B that you had for the first measurement, and record the parameters again.

Calculate the output admittance,

$$h_{oe} = [\Delta I_E / \Delta V_{CE}] \text{ constant } I_B,$$

and the reverse voltage ratio,

$$h_{re} = [\Delta V_{BE} / \Delta V_{CE}] \text{ constant } I_B.$$

Typical values for these parameters are $h_{oe} \sim 10^{-4}$ S and $h_{re} \sim 5-10 \times 10^{-4}$.

- The input impedance of the transistor (h_{ie} or r_{in}) can be measured as follows. Keeping V_{CE} constant (at -8 V for example) set I_B to $6 \mu\text{A}$ and then $10 \mu\text{A}$, and record the values of I_E and V_{BE} at each point. Calculate h_{ie} for your transistor from:

$$h_{ie} = [\Delta V_{BE} / \Delta I_B] \text{ constant } V_{CE}$$

A typical value for this parameter is $3.5 \text{ k}\Omega$.

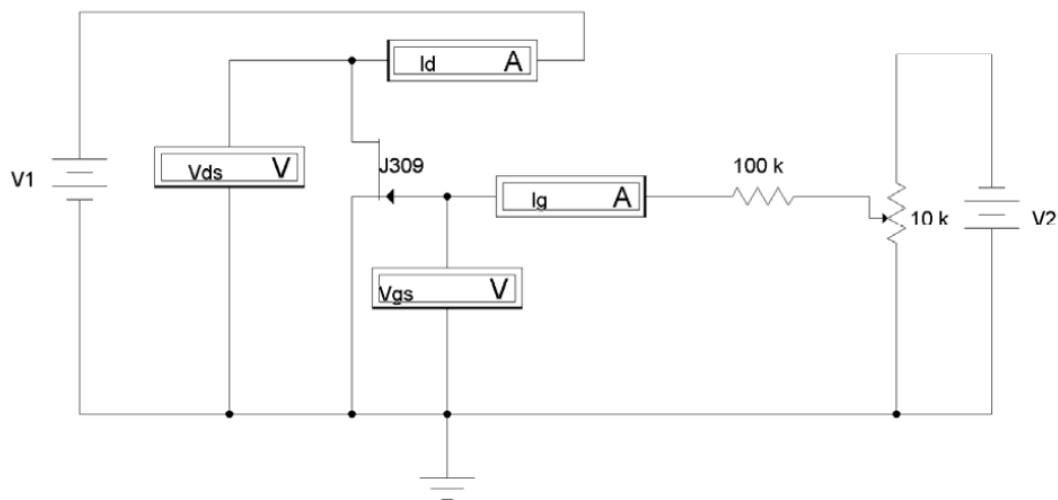
- As discussed in class, the input impedance is related to h_{fe} (or β) and a quantity called the transresistance according to $r_{in} = h_{fe} r_{tr}$. Calculate $h_{fe} = \Delta I_E / \Delta I_B$ from the measurements taken in step 4 and determine the transresistance. Compare your result with the calculated transresistance, $r_{tr} = 26 \text{ mV} / I_E$ where I_E is the average of the two values from step 4.
- Using the transistor curve tracer, measure the collector characteristics of your transistor. The curve tracer generates a plot of I_C vs V_{CE} for several values of I_B . The Appendix to this experiment describes how to set up the curve tracer for bipolar transistors and FET's. Make a copy of the curve tracer output and tape the picture in your notebook. Label the axes with the name of the quantity plotted and also indicate the scale. Label each curve with the appropriate value of I_B .

From the curve tracer plot determine the value of β for $I_B = 20 \mu\text{A}$ and $V_{CE} = -12 \text{ V}$. Compare the result with the value you got in step 1.

II. THE FIELD EFFECT TRANSISTOR

In this section we will measure some of the properties of an n-channel junction field-effect transistor (model J309).

1. Use the transistor curve tracer to obtain a plot of the drain characteristics for the FET. The curve tracer plots I_D vs V_{DS} for several values of V_{GS} . Make a copy of the curve tracer output, tape it in your notebook, label the scales, and indicate the appropriate value of V_{GS} for each curve. The characteristics of a given FET can vary widely from the “typical” values given in the Appendix to this experiment. Before going on to step 2, consult with your instructor to see if the procedure given below needs to be modified for the particular FET you are using.



Set the circuit board as shown in the diagram above. For an FET the gate and drain voltages must have opposite signs, and therefore we need to use two power supplies.

Start by turning the 10 kΩ pot fully CCW. Ground the positive terminal of the V_1 supply and the negative terminal of the V_2 supply. As in section I, we will use VOM's to measure the current, and digital meters to measure the voltages. After making all the connections, turn on the power supply and set V_2 to about 8 volts.

2. An FET can be used as a “variable resistor”, in which the resistance of the drain-source channel is adjusted by varying the gate voltage, V_{GS} . In this step we will measure the resistance of the channel for $V_{GS} = 0$.

With the pot fully CCW you should get $V_{GS} = 0$. Vary V_{DS} (by adjusting V_1) from 0 to -2.0 V in 0.2 V steps, and make a plot of I_D vs V_{DS} . Determine

the drain-source resistance, R_{DS} , from the ohmic (linear) region of the plot.

From the curve tracer plot generated in step 1, determine whether R_{DS} increases or decreases when the gate voltage is decreased.

3. Next we will measure some of the characteristics of the FET in the “pinch-off” region. In this region I_D is essentially independent of V_{DS} (i.e. the transistor acts like a constant current source). This is the region where an FET can be used as an amplifier.

Set V_{GS} to 1.5 V by adjusting the 10 k Ω pot, and then vary V_{DS} from -2 V to -20 V in 2 V steps. As you make the measurements notice that (as expected) the gate current is essentially zero. Make a plot of I_D vs V_{DS} .

For a constant current source, the output impedance should be large. Determine the output impedance of the FET in the pinch-off region,

$$r_{0S} = \Delta V_{DS} / \Delta I_D ,$$

by using your measurements at $V_{DS} = -10$ V and -20 V.

4. FET's are sometimes used as switches or gates. The switch is closed when $V_{GS} = 0$ and open when V_{GS} exceeds some cutoff value $V_{GS(off)}$. With $V_{DS} = -12$ V, vary the pot to change the gate-source voltage, V_{GS} . Measure and tabulate I_D as a function of V_{GS} for $V_{GS} = 0$ V to the cutoff voltage using 0.5 V steps for V_{GS} (you may want to adjust V_1 at each step to maintain $V_{DS} = -12$ V). Plot I_D vs V_{GS} (the graph should be approximately parabolic) and determine the cutoff voltage.

APPENDIX: PROPERTIES OF THE TRANSISTORS USED IN THIS EXPERIMENT

The silicon planar epitaxial signal 2N3904 (NPN) and 2N3906 (PNP) transistors have nearly identical characteristics. They constitute a complimentary pair. The table below gives some important characteristics and the standard symbols. Unless otherwise noted, the values are the maxima at 25 C.

Voltages		
Collector-Emitter	V_{CEO}	40 V
Collector-Base	V_{CBO}	60 V
Emitter-Base	V_{EBO}	5 V
Current		
Collector	I_C	200 mA
Dissipation	P_T	200 mW
Cutoff Current		
Collector	I_{CEV}	50 nA
Base	I_{BEV}	50 nA
Saturation Voltage		
Collector-Emitter	$V_{CE(SAT)}$	0.20 V
Base-Emitter	$V_{BE(SAT)}$	0.85 V
Forward Current Transfer Ratio		
$I_C = 1 \text{ mA}$	h_{fe} or β	100 typical
$I_C = 10 \text{ mA}$		200 typical
Capacitance		
Collector-Base	C_{cb}	4.5 pF
Emitter-Base	C_{eb}	10 pF

The J309 is an RF amplifier small signal N-Channel Depletion Mode JFET.

Voltages		
Drain-Source	V_{DS}	25 V
Gate-Source	V_{GS}	-25 V
Gate-Source Cutoff	$V_{GS(off)}$	-1.0 V Min -4.0 Max
Currents		
Gate Reverse	I_{GSS}	-1.0 nA Max
Zero-Gate Voltage Drain	I_{DSS}	12 mA Min 30 mA Max
Forward Transconductance	g_{fs}	20 mS
Input Capacitance	C_{iss}	5 pF

CURVE TRACER APPENDIX

The table below indicates the appropriate Curve Tracer settings.

	2N3904	2N3906	J309
Collector Sweep or Drain Sweep (FET)	20 V	20 V	20 V
Current Sensitivity (Signal)	10 mA/V	10 mA/V	10 mA/V
Selector	Transistor	Transistor	FET
Polarity	NPN	PNP	N Channel
Base Current or Gate Voltage	10 μ A/step	10 μ A/step	0.5 V/step