Use '193 LOAD' input to pin counter to load value during times when this state has not been selected by the TOP-level FSM. When the state is selected the LOAD' is pulled high for the period of that state. The counter counts until decrementing through 0 when BO' is asserted for 1/2 (!!) clock cycle. This is actually unfortunately limiting the maximum CLK frequency of this circuit to about 2.5 MHz.
DSTM1
Implementation = DS_RST

DSTM2
Implementation = DS_S1

DSTM3
Implementation = DS_S2

DSTM4
Implementation = DS_S3

OFFTIME = .2u
ONTIME = .2u
DELAY = 0
STARTVAL = 0
OPPVAL = 1

S1
Implementation = DS_S1

S2
Implementation = DS_S2

S3
Implementation = DS_S3

CLK
STMCLK1
OFFTIME = .2u
ONTIME = .2u
DELAY = 0
STARTVAL = 0
OPPVAL = 1

VCC

5V

0

V1

DSTM2
Implementation = DS_S1

DSTM3
Implementation = DS_S2

DSTM4
Implementation = DS_S3