Formation of regular step arrays on Si(111)7×7

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Highly regular arrays of steps are produced on vicinal Si(111)7×7 surfaces. A tilt of the surface normal from (111) toward (1 1 2) produces single steps (0.3 nm high and typically 15 nm apart). The opposite tilt toward (1 1 2) produces bunched steps with adjustable height (1–5 nm) and a spacing of 70 nm. Preparation criteria for straight edges and regular spacings are determined, taking into account the miscut angle (azimuthal and polar), annealing sequence, current direction, and applied stress. © *1998 American Institute of Physics.* [S0021-8979(98)04113-9]

INTRODUCTION

In recent years, it has become possible to design and fabricate nanostructures[1] in a controlled way. An appealing technique is self-assembly of nanostructures, which avoids the complications of nanolithography and the slow speed of nanowriting. Here we are interested in one-dimensional structures, such as arrays of wires and stripes. In this case it is useful to have an array of steps at a vicinal surface, which can be used as template for producing stripes by decorating the step edges in a step-flow growth mode.[2–6] Thereby, the stripe width and the stripe spacing can be controlled independently by the coverage and the tilt angle of the vicinal surface, respectively. More general schemes have been proposed, where a set of passivating stripes acts like the photoresist in microlithography.[6] That allows the combination of materials that do not exhibit a step flow growth mode, such as reactive metals on silicon. It also should makes it easier to obtain stripes thicker than a monolayer by selective deposition on the part of the substrate not covered by the passivating stripes.

For all these structures it is essential to start out with smooth steps. Silicon, of course, is among the preferred substrates. There have been extensive studies of steps and kinks on silicon, including their kinetics and dynamics.[7–17] Our goal is to utilize the lessons from this work to optimize silicon substrates for step flow growth of quantum wires. In particular, we want to avoid kinks in order to obtain the smoothest possible step edges and wires. Recently, we have reported highly perfect single steps.[18] In the following, we give a more detailed account of regular step arrays on silicon that includes bunched steps in addition to single steps.

Our choice of Si(111)7×7 as the substrate is motivated by the existence of a particularly stable step geometry on this surface. The top edge of an equilibrated step consists of a string of corner holes of the 7×7 unit cell,[6–10] running along the $[\bar{1}10]$ direction. Thereby, the 7×7 reconstruction helps ordering the step arrays by quantizing the terrace width in units of half the 7×7 unit cell (2.3 nm).[14] This still leaves us with two possible orientations of the step edge, where the surface normal is tilted from (1 1 1) towards opposite directions, i.e., (112) and (112). The steps with the (112) tilt are taken as the most stable configuration since they are found to occur during Si-on-Si(111) epitaxy.[7] The Si(100)2×1 surface has a more complex step structure consisting of alternating rough and smooth steps, which do not easily combine into smooth double steps.

We are able to produce highly regular step arrays on Si(111)7×7. Kink densities as low as one in $2\cdot10^4$ lattice sites are achieved. Single steps (0.31 nm high) are observed for a tilt of the surface normal from (111) toward (1 12). A tilt toward (112) produces bunched steps with a spacing of about 70 nm. Their height can be tailored by the miscut angle from five steps per bunch (1.6 nm total height) at a 1.3° miscut angle to 14 steps per bunch (4.4 nm total height) at a 3.5° miscut. Several parameters are considered for perfecting the step arrays, such as miscut angle (azimuthal and polar), annealing sequence, current direction, and external stress. The optimum annealing sequence consists of several steps that circumvent undesirable regions of the surface phase diagram.

EXPERIMENTAL METHOD

We studied Si(111) wafers with miscuts between 1° and 4° along (1 12) and (112), respectively. The doping was *n*-type in the 10^{18} cm^{-3} range. They were held as stress-free as possible between Ta wire loops and heated by a dc current parallel to the direction of the step edges. This avoids electromigration effects[16] complicating the surface morphology. The temperature was determined by a Minolta-Land Cyclops 52 optical pyrometer with the emissivity set to 0.4. We estimate the temperature uncertainty to be ±30°.

Arrays of single steps were obtained from samples cut 1.1° towards (1 12) using a multi-stage annealing sequence. The wafers were outgassed for $\frac{1}{2}$ h by raising the temperature slowly up to 700 °C, flashed to 1260 °C for 10 s to diffuse residual surface carbon into the bulk, and cooled to 1060 °C in 1 min, where single steps are stable. The most critical part

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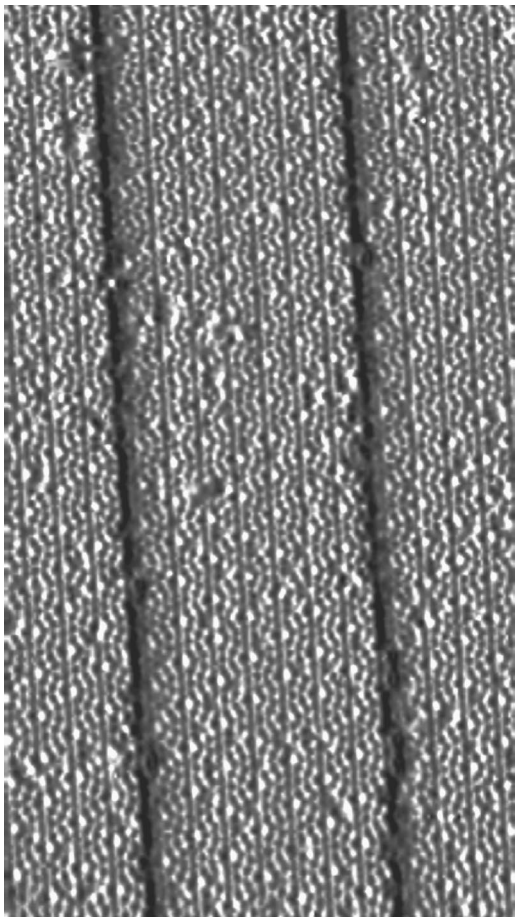

FIG. 1. STM image of two steps (dark lines) for a Si(111)7×7 surface tilted 1.1° toward (1 12), with the step edges parallel to the [110] direction. Rows of 7×7 corner holes form the upper edges and appear as grooves on the terraces. Their spacing is 2.3 nm (half of the 7×7 unit cell). The *x*-derivative of the topography is shown, producing a side-illumination effect where light incident from the left casts shadows down the steps to the right. The same holds for Figs. 2–6. 40×70 nm^2.

is a quench to 850 °C within 3 s for avoiding a step tripling regime, and a slow ($\frac{1}{2}$ h) cool-down from 850 °C for developing long-range 7×7 domains and kink-free step edges.

Arrays of bunched steps were obtained for a miscut in the opposite direction, i.e., towards (112). For small miscuts, such as 1.3°, we used the heating sequence described above. Step-bunching on these surfaces is spontaneous. At surfaces with higher miscut the bunching process slows down, requiring a modified annealing sequence beyond the 1060 °C point. From there on, the sample was cooled slowly, instead of quenched, proceeding from 1060 °C to 650 °C at a rate of 0.5 °C/s or slower. This allowed the surface to establish a quasi-equilibrium state during cooling, which was essential for the development of regular arrays of the bunched steps.[19] A 30 min post-anneal at 650 °C was applied to permit the bunched steps to reach a self-limited maximum size reported previously.[11,19,20]

Scanning tunneling microscope (STM) images were taken at a tunneling current of 0.4–0.8 nA and a sample bias of +2 V. In order to enhance the steps, the derivative of the topography in the *x*-direction is presented in all STM images. It can be viewed as the surface illuminated from the left side with the steps dropping off toward the right.

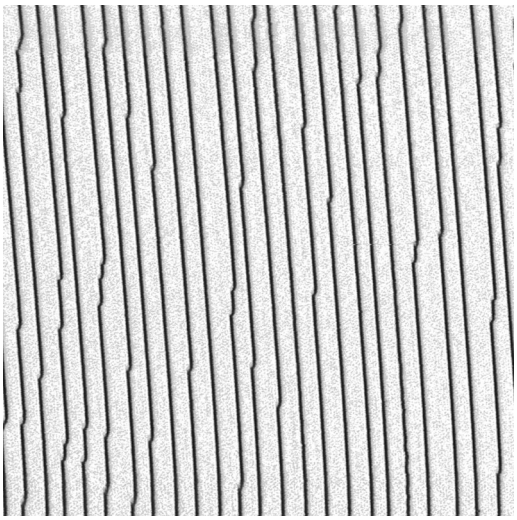

FIG. 2. Array of steps and kinks on a Si(111)7×7 surface tilted 1.1° toward (1 12), showing a quantization of the kink width in units of 2.3 nm. A slight azimuthal misorientation of 1° gives rise to kinks. 340×340 nm^2.

SINGLE STEPS

Figures 1–3 show STM images from step arrays on a Si(111)7×7 surface, miscut by 1.1° toward (1 12). Figure 1 gives a close-up of the step and terrace structure, containing two atomically straight steps running along the [110] direction and three terraces with single-domain 7×7 reconstructions. The steps are one Si(111) double-layer high (0.31 nm). The average terrace width of 15 nm corresponds closely to the nominal miscut of 1.1°. In Fig. 2, a larger area is shown which contains atomically straight step sections interrupted by a series of kinks. All kinks have an identical width[18,21] of 2.3 nm. They all point to the right and are, on average, 470

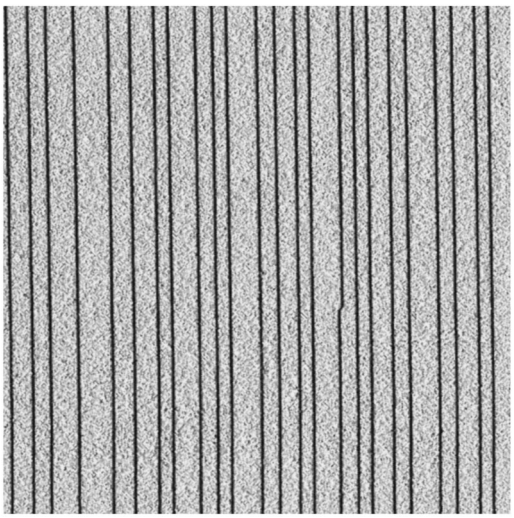

FIG. 3. Step array on a Si(111)7×7 surface similar to that in Fig. 2, but without the azimuthal misorientation. The image contains a single kink in 2×10^4 step edge sites, located on the ninth step from the right. 340×390 nm^2.

lattice spacings apart. These kinks are created by a small miscut in the azimuthal direction, about 1° away from (1 12). To reduce the kink density we have searched for spots on the Si wafer with the correct azimuthal orientation, such as in Fig. 3. A lone kink is observed in this image, over an area that comprises $2 \cdot 10^4$ step edge sites.[18] This kink density is significantly lower than the upper limit of one in 10^2 sites set for H-terminated Si(111) surfaces.[16] The steps on Si(111)7 $\times$7 are much smoother than those obtained on metal surfaces.[5]

Such a low kink density can be achieved because of the long-range 7×7 reconstruction of the surface. For the stable step orientation, the upper edge of a step passes through the corner holes of the 7×7 unit cells.[6–10] These rows of corner holes can be seen in Fig. 1 as vertical grooves. A kink has to be at least one row spacing wide (2.3 nm) to jump from one row to the next. This is true as long as the 7×7 reconstruction remains single-domain on a given terrace, which we achieve by careful annealing. The large size of a minimum kink provides a high energetic and kinetic barrier for kink creation[10,13] and explains the smoothness of the step edges observed on Si(111)7×7.

BUNCHED STEPS

Figures 4(a),(b) are STM images of bunched steps on Si(111)7×7 surfaces miscut towards (112) by 1.3° and 3.5°, respectively. Light areas are atomically flat 7×7 terraces, dark areas contain bunched steps, which are resolved in more detail in Figs. 5(a),(b) and 6. Both miscuts exhibit a comparable periodicity, i.e., the total width of the light and dark areas in the images (70 ± 10 nm for the 1.3° sample and 75 ± 10 nm for the 3.5° sample). These results are consistent with a previously reported[20] saturation of the spacing between facets at about 70 ± 10 nm for long annealing times, which has been attributed to the elastic relaxations caused by the facet edges. The different average miscut is reflected in the different height of the bunched steps. A close-up of these step bunches in Figs. 5(a),(b) resolves them into individual Si(111) steps, each 0.31 nm high. There are 5 ± 1 steps per bunch for the 1.3° miscut [Fig. 5(a)] and 14 ± 1 steps per bunch for the 3.5° miscut [Fig. 5(b)]. In both cases, the narrow ledges between single steps are about 2.4 nm wide, giving an inclination angle of $\approx7°$ for the regions with bunched steps. Note that this angle is exaggerated in the line scans of Figs. 5(a),(b), due to the difference in the vertical and horizontal scales. The inclination angle of the step bunches is independent of the miscut of the sample for the miscut angles from 1° to 4° studied here, suggesting a stable facet structure. At a higher miscut of 10°, a steeper inclination angle of 22° has been reported,[22] corresponding to a (331) facet. To test whether we have a well-defined structure on our 7° facet, we have examined it more closely on the 3.5° miscut sample (Fig. 6). The narrow (111) ledges between individual steps are reconstructed with patches of adatom arrangements similar to the 5×5 analog of the 7×7 reconstruction. Again, the top edges of the steps are formed by rows of corner holes. This is similar to the step structure found for the single-height steps on miscuts toward (1 12),

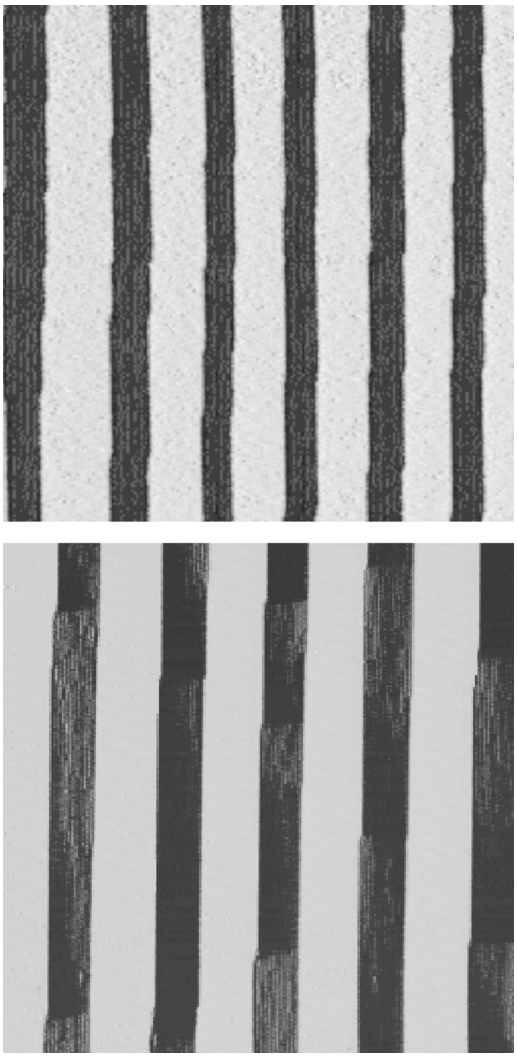

FIG. 4. Bunched steps on two Si(111)7×7 surfaces tilted toward $(11\bar{2})$. The light stripes are flat 7×7 terraces, the dark regions correspond to bunched steps. 380×380 nm^2. (a) Tilt angle 1.3°. (b) Tilt angle 3.5°.

even though the uphill and downhill directions are interchanged. In both cases, the stability of a step edge consisting of corner holes leads to a low kink density. Each ledge on the 7° facet is about 2.4 nm wide, slightly larger than half a unit cell of the 7×7 reconstruction (2.3 nm). Thus the 7° facet represents the tightest possible array of single steps that preserves the terrace width quantization, containing just a single 7×7 quantum per terrace.

ANNEALING STRATEGY

The driving forces underlying facet growth of vicinal Si(111) surfaces have been studied in previous work by various authors.[11,23,24] These findings help us choosing the optimum annealing sequence for obtaining either single-height or bunched steps. In Fig. 7, we show a schematic diagram of the prevalence of various step structures versus temperature and miscut, based on previous work[11,19,22] and on our own results. It contains a nearly horizontal boundary where the 1×1 structure (upper region) is transformed to the 7×7 reconstruction (lower region).[19,22,25] Below the phase boundary, three different regions are marked: triple steps, single

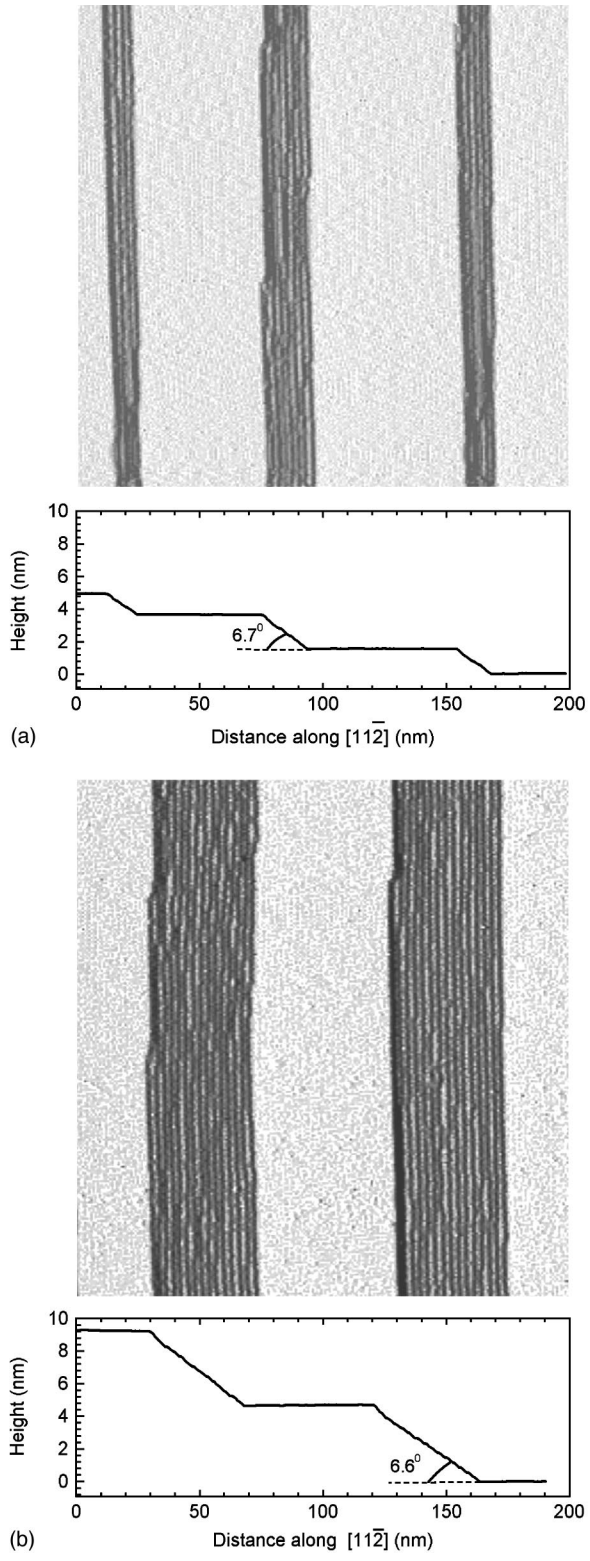

FIG. 5. Detail of the two Si(111)7×7 surfaces with bunched steps in Fig. 4(a),(b), including a line scan across the steps. The height of the step bunches is proportional to the miscut angle, while the periodicity is nearly constant. 200×200 nm^2. (a) Tilt angle 1.3°. (b) Tilt angle 3.5°.

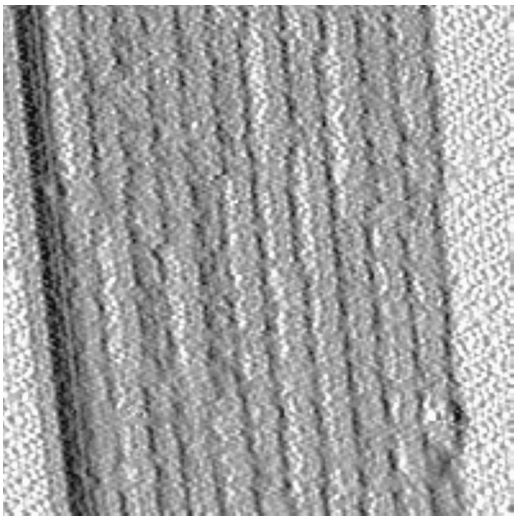

FIG. 6. Close-up image of a step bunch for the surface in Figs. 4(b), 5(b). The ledges between individual steps exhibit patches of a 5×5 adatom reconstruction. 38×38 nm.

steps, and step bunches. The arrows represent our cooling pathways, the solid circles post-annealing. In the following, we will discuss how our heating sequences can be rationalized from this diagram. In general, four parameters are relevant in producing highly regular single-height steps:[18] miscut angle, annealing temperature and time, heating current direction, and stress. All are optimized for producing regular arrays of steps. Particularly important are two factors, that is the cooling rate and the post-annealing temperature. Rapid quenching through step bunching regions allows us to preserve the single-height steps that are stable at high temperature. Slow cooling near thermal equilibrium allows step bunches to form. Post-annealing at temperatures in the 7×7 regime smoothens out step edges and produces single-domain 7×7 terraces. It also drives bunched steps to reach a self-limited size.

To create regular single-height steps, we use samples with a small miscut toward (1 12). At a miscut of $\leqslant 2°$ single-height steps are predominant[25] at temperatures well below the 1×1 to 7×7 phase transition (860 °C), as indicated in Fig. 7. Right at the phase transition a minor fraction of triple-height steps forms on these surfaces (8% at a 1.2°

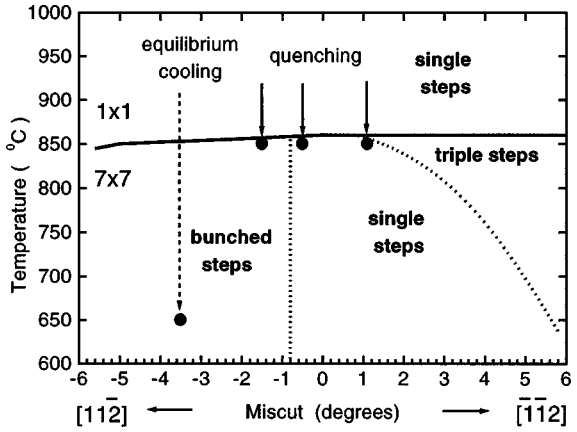

FIG. 7. Qualitative diagram of the prevalence of various step structures on vicinal Si(111) surfaces, including the 7×7 to 1×1 phase transition (see Refs. 11, 19, and 20) and regions of single, triple, and bunched steps. The arrows and solid circles indicate the annealing sequences and post-anneal temperatures used for obtaining regular step arrays.

miscut).[11] These triple steps quickly become immobile when lowering the temperature and cannot be removed by post-annealing. Therefore, we choose to quench the sample through the narrow temperature window where the tripling of the step height occurs, effectively eliminating triple steps. Longer annealing at temperatures below this window permits the development of the long-range, single-domain 7×7 terraces which remove the kinks on the step edges and stabilize the step configuration.[18] A post-annealing time of 30 min at 850 °C is found to significantly reduce the number of the kinks at the step edges. For temperatures below 800 °C, the mobility of the Si surface atoms becomes too small to improve the long range order. Significantly longer time was required to achieve any additional ordering at an annealing temperature of 700 °C, as reported previously.[11]

To obtain a regular array of bunched steps, we choose samples miscut toward the (1 1 2) azimuth, where the coexistence of $(111)7\times7$ facets and bunched steps represents the equilibrium morphology. This faceting has been attributed to the orientation dependence of the surface free energy.[11,20] Within the step bunching region we have established two different annealing procedures, depending upon the miscut angle. For a small ($<2°$) miscut toward (112) we find spontaneous formation of a stripe pattern where $(111)7\times7$ facets alternate with facets consisting of step-bunches. This step-bunching instability has been ascribed to a long-range attractive interaction between steps, which is produced by elastic relaxation.[23] By quenching from temperatures above the 1×1 to 7×7 transition we allow limited numbers of steps with high bunching rate to cluster into one bunch. Empirically, a narrow distribution of the size of the bunched steps is obtained. With slower cooling we find ''free'' steps between the ordered bunches of 4–5 steps, possibly influenced by the competing factors that lead to simultaneous bunching and debunching.[24]

On samples with higher miscut [$>2°$ toward $(11\bar{2})$], the step density increases such that the short-range repulsive interaction between steps becomes important.[11,23,26] That slows the initial step-bunching rate significantly.[23] At the same time, it requires lower temperatures to further lower the surface free energy driving larger number of the steps to coalesce.[20,26] Therefore, we have to use a slower cooling rate and lower post-annealing. To form a cluster of 14 steps on the 3.5° miscut surface requires tens of seconds at 850 °C, at least 10 times longer than what is needed for a cluster of five steps on the 1.3° miscut sample.[20,23] We choose to cool down the surface with a rate less than 0.5 °C/s while passing through the 1×1 to 7×7 phase transition. This cooling rate is sufficient to allow the surface to reach the steady state in the temperature range where step-bunching occurs.[11] In contrast, only few steps become bunched during fast cooling, leading to poorly ordered step bunches with a high density of kinks. Steps continue to coalesce as the temperature decreases.[11,20] We find that post-annealing at a temperature as low as 650 °C for at least 30 min is required gives rise to a regular array of bunched steps separated by uniform $(111)7\times7$ facets. Annealing for the same time at higher temperatures (750 °C) never creates a surface with this regularity. Symptoms appear that are similar to those observed upon fast cooling: either the steps are not closely packed, or the step bunches contain only 7–8 steps, instead of the maximum size of about 14 steps obtained at the lower temperature of 650 °C for a 3.5° miscut. In summary, long post-annealing is required for obtaining regular and self-limited step bunches, using temperatures below the 1×1 to 7×7 phase transition.

SUMMARY AND OUTLOOK

Highly-perfect step arrays can be produced on tilted $Si(111)7\times7$ surfaces by a proper choice of the wafer miscut and by an annealing sequence that passes quickly through undesirable regions of the surface phase diagram. The kink density can be as low as $5\cdot10^{-5}$ per lattice site, making $Si(111)7\times7$ steps ideal for creating quantum wires[2,3,5,18] by growth along atomically straight steps. We are in the process of fabricating such structures, e.g., epitaxial $CaF_2(111)$ stripes[27] that can play the role of a photoresist in traditional microlithography. Regular arrays of bunched steps can be produced as well, choosing a miscut orientation opposite to that for single steps. Their step height can be controlled by the miscut angle. Step bunches might be useful for creating coarser nanowires, e.g., by side evaporation.[28] Such sawtooth structures might become useful for producing structures exhibiting giant magnetoresistance (GMR) in the more-efficient CPP geometry (current perpendicular to the plane).[2]

ACKNOWLEDGMENTS

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