Atomic scale memory at a silicon surface

R Bennewitz[1,2]**, J N Crain**[1]**, A Kirakosian**[1]**, J-L Lin**[1]**,
J L McChesney**[1]**, D Y Petrovykh**[1] **and F J Himpsel**[1]

[1] Department of Physics, UW-Madison, 1150 University Ave., Madison, WI 53706, USA
[2] Department of Physics and Astronomy, University of Basel, 4056 Basel, Switzerland

Abstract
The limits of pushing storage density to the atomic scale are explored with a
memory that stores a bit by the presence or absence of one silicon atom.
These atoms are positioned at lattice sites along self-assembled tracks with a
pitch of five atom rows. The memory can be initialized and reformatted by
controlled deposition of silicon. The writing process involves the transfer of
Si atoms to the tip of a scanning tunnelling microscope. The constraints on
speed and reliability are compared with data storage in magnetic hard disks
and DNA.

1. Introduction

In his landmark 1959 talk at Caltech, Richard Feynman
estimated that 'all of the information that man has carefully
accumulated in all the books in the world, can be written . . . in a
cube of material one two-hundredth of an inch wide'. Thereby,
he uses a cube of $5 \times 5 \times 5 = 125$ atoms to store one bit, which
is comparable to the 32 atoms that store one bit in DNA. Such
a simple, back-of-the-envelope calculation gave a first glimpse
into how much room there is for improving the density of stored
data when going down to the atomic level. In the meantime,
there has been great progress towards miniaturizing electronic
devices all the way down to single molecules or nanotubes
as active elements [1]. Memory structures have been devised
that consist of crossed arrays of nanowires linked by switchable
organic molecules [2, 3] or crossed arrays of carbon nanotubes
with electrostatically switchable intersections [4].

It is our goal to push the storage density to the atomic
limit and to test whether a single atom can be used to store a
bit at room temperature. How closely can the bits be packed
without interacting? What are the drawbacks of pushing the
density to its limit while neglecting speed, reliability and ease
of use? The result is a two-dimensional realization of the
device envisaged by Feynman, as shown in figure 1. A bit is
encoded by the presence or absence of a Si atom inside a unit
cell of $5 \times 4 = 20$ atoms. The remaining 19 atoms are required
to prevent adjacent bits from interacting with each other, which
is verified by measuring the autocorrelation. A specialty of
the structure in figure 1 is the array of self-assembled tracks
with a pitch of five atom rows that supports the extra atoms.
Such regular tracks are reminiscent of a conventional CD-
ROM [5]. However, the scale is shrunk from μm to nm, which
corresponds to a million times higher density. The readout of
such a memory via scanning tunnelling microscopy (STM) is
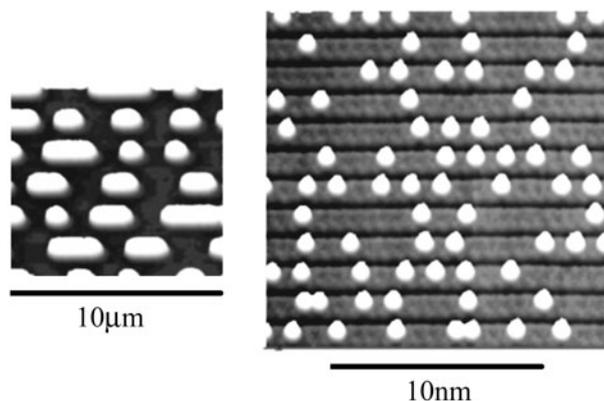
Figure 1. Comparison of the atomic memory on silicon with a
CD-ROM [5]. Extra silicon atoms occupy lattice sites on top of
tracks that are five atom rows wide (1.7 nm). The scale is reduced
from μm to nm, which leads to a 10^6 times higher density.

obvious, albeit slow. Writing is more difficult. While atoms
can be moved controllably at liquid helium temperature [6], it
is much harder to achieve that at room temperature [7–14]. In
order to prevent diffusion, it is necessary to choose atoms that
are strongly bound to the surface. Moving them requires strong
forces and a close approach by the STM tip, which entails the
risk of an atom jumping over to the tip. We use this effect as
virtue to remove a silicon atom from the surface for writing
a 0. The memory is pre-formatted with a 1 everywhere by
controlled deposition of silicon onto vacant sites.

In the following we begin with a description of the memory
structure, move on to writing and reading, and eventually
explore reliability and speed. The outlook considers the
fundamental limitations of a single atom memory and makes
a comparison to data storage in DNA.

2. Memory structure

The self-assembled memory structure shown in figures 1 and 2 is obtained by depositing 0.4 monolayers of gold onto a Si(111) surface at 700 °C with a post-anneal at 850 °C, thereby forming the well-known Si(111)5 × 2–Au structure [15–17]. All images are taken by STM with a tunnelling current of 0.2 nA and a sample bias of −2 V. At this bias the extra silicon atoms are enhanced compared to the underlying 5 × 2 lattice. A stepped Si(111) substrate tilted by 1° towards the [$\bar{1}\bar{1}2$] azimuth is used to obtain one of the three possible domain orientations exclusively [17]. The surface arranges itself into tracks that are exactly five atom rows wide (figure 1, right). They are oriented parallel to the steps in the [$\bar{1}$10] direction. Protrusions reside on top of the tracks on a 5 × 4 lattice. Only half of the possible sites are occupied in thermal equilibrium (figure 2(a)). When varying the Au coverage the occupancy remains close to 50%. Excess Au is taken up by patches of the Au-rich Si(111)$\sqrt{3} \times \sqrt{3}$–Au phase, and Au deficiency leads to patches of clean Si(111)7 × 7. In order to find out whether the protrusions are Si or Au, we evaporate additional Si and Au at low temperature (300 °C). Silicon fills the vacant sites (figures 2(b) and (d)), but gold does not. In figure 2(b) the occupancy of the 5 × 4 sites has increased to 90 ± 3% from 53 ± 4% in figure 2(a). Higher annealing allows the extra Si to diffuse away to the nearest step and causes vacancies to reappear, confirming that the half-filled structure is thermodynamically stable. Thus, an average code with 1 and 0 in equal proportion is particularly stable.

The writing process consists of removing Si atoms from a nearly filled lattice, such as that in figures 2(b) and (d). Figure 3 demonstrates one of two methods, which is based on chemical attachment to the tip. The tip is brought down towards the Si atom to be removed, typically by 0.6 nm for 30 ms without applying a voltage. This method is similar to previous work on Ge(111), where 98% reliability has been achieved in removing a single atom [13]. A less reliable method uses field desorption by a voltage pulse of −4 V on the sample (30 ms long) with the tip hovering above the Si atom to be removed.

The readout is demonstrated in figure 2(e). A line scan along one of the tracks in figure 2(c) (marked by an arrow) produces well-defined peaks for extra Si atoms that protrude well beyond the noise level. Since the memory is self-formatted into tracks it can be read by a simple, one-dimensional scan. There is no need to search in two dimensions for the location of a bit. The signal is highly predictable since all atoms have the same shape and occur on well-defined lattice sites. After subtracting identical Gaussians at the lattice sites one obtains a residual comparable to the noise (figure 2(e) bottom trace). The height of the signal ($z = 0.13$ nm) exceeds the noise ($\delta z = 0.005$ nm rms) by a factor of 26, using a dwell time of 500 μs/point. A highly reproducible pulse shape allows sophisticated signal filtering techniques because most noise signals do not match the known shape and can be removed. An example is partial response maximum likelihood detection (PRML), which is widely used for the readout of magnetic hard disks [18–20] and in long-distance communications. In PRML the signal is filtered to produce a standard line shape, sampled at regular intervals and processed in real time by the Viterbi algorithm, which selects the most likely bit sequence.
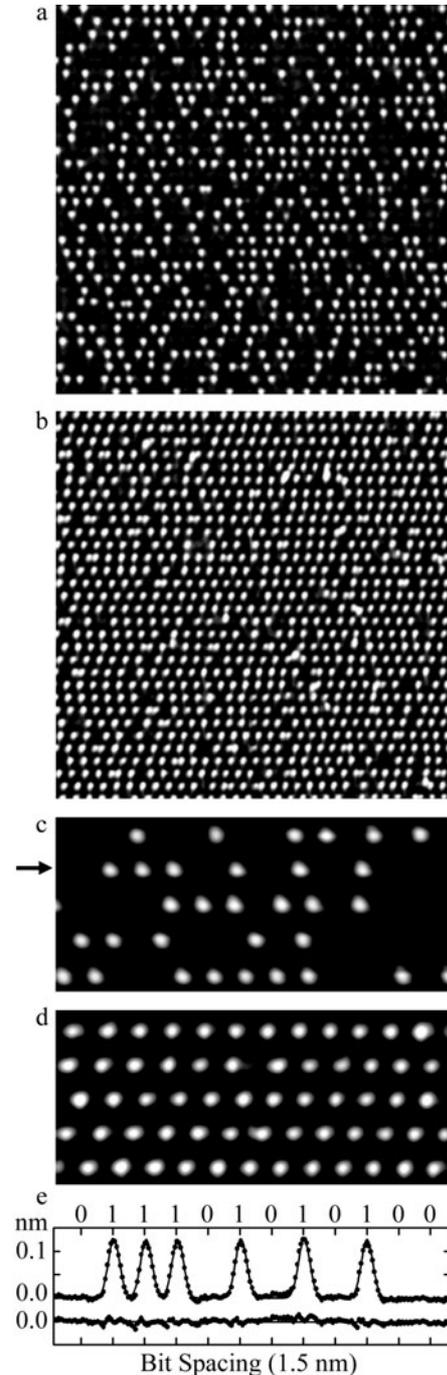
Figure 2. STM images of the equilibrium structure with half filling of the atomic sites (a), (c) and the pre-formatted structure with nearly complete filling (b), (d). A line scan with 500 μs dwell time per point is shown in (e), following the arrow in (c). Identical peaks have been subtracted at the lattice sites of the Si atoms in the bottom curve to demonstrate a highly reproducible signal.

3. Reliability and speed

Reliability becomes a key issue with such a small memory cell. The writing process is too slow and error prone to be practical, but the readout deserves closer inspection. Our data provide quantitative input for determining the achievable error rate, the thermal stability and correlations between adjacent bits.
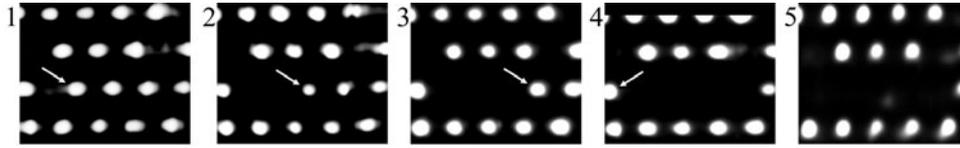
Figure 3. Writing a sequence of four zeros. Silicon atoms are transferred to the STM tip one by one (arrows).

The error rate for reading is related to the effective signal-to-noise ratio (SNR), which is determined by three input parameters for hard disk readout using PRML [18]:

$$\text{SNR} = 2/\pi W B/\sigma^2$$

W is the full width half maximum of a signal pulse, B the bit spacing and σ the variance in the jitter of the pulse positions. Typical values for hard drives [19] are $W \approx 120$ nm, $B \approx 50$ nm, $\sigma \approx 4$ nm, giving SNR $\approx 240 \approx 24$ dB and an error rate of 10^{-8}. For the atomic memory one can derive analogous quantities $W = 0.55$ nm, $B = 1.54$ nm, and $\sigma = 0.015$ nm from figure 2(e) by taking the peak width, the lattice spacing and the jitter of the peak positions relative to the lattice points (from Gaussian fits with unconstrained positions). These numbers can serve as input for designing filters and codes that minimize the error rate. Such models will be different from those for hard disks, where readout pulses alternate in sign and bits are less than a pulse width apart. A closer analogue might be the unipolar soliton pulses that are used in long distance communications through optical fibres. Pulse amplitude variation plays a role for solitons, which is 0.005 nm or 4% of the peak height in our case.

The thermal stability of Si atoms on the tracks can be estimated by fitting high-temperature STM results from [15] to a simple model of activated diffusion. The temperature dependence of the jump rate $\nu(T)$ is determined by a Boltzmann factor containing an activation energy ΔE:

$$\nu(T) = \nu_0 \exp(-\Delta E/k_B T).$$

The attempt frequency ν_0 is comparable to the frequency of lattice vibrations, with a typical value $\nu_0 = 10^{13}$ s^{-1}. Estimating a jump rate of about 1 s^{-1} at a temperature $T =$ 475 K from the data in [15] one obtains an activation energy $\Delta E = k_B T \ln(\nu_0/\nu) \approx 1.2$ eV. That gives a jump rate of 10^{-8} s^{-1} at room temperature ($k_B T = 25$ meV), i.e. one jump in 2–3 years. Thus, thermal stability is not an issue compared to less fundamental limits, such as surface contamination.

Correlations between adjacent bits come into play at high storage density. In magnetic storage one has to be concerned about magnetic coupling between adjacent particles at a bit spacing of 10 nm or less [20–22]. The bits are much closer than that on the Si surface (1.5 nm along the track and 1.7 nm between tracks). In order to detect interactions between the Si atoms we have determined the autocorrelation function of their equilibrium distribution (figure 4). Along the tracks, the nearest site of the underlying 5×2 lattice is almost completely excluded, with an occupancy of only 0.04 relative to the average (figure 4 (bottom), compare [16]). Therefore, a bit spacing of 2 lattice sites would discriminate a 1 1 pair against a 1 0 by a factor of 25. All other correlations are much closer to the average of 1, with the largest deviation (1.33) occurring at the second 5×2 site in figure 4 (bottom). Thus, the 5×4 cell represents the smallest viable cell for the underlying 5×2 lattice that keeps bit interactions under control. Feynman's proposed spacing of five atoms between bits was correct.

One of the fundamental limitations to devices operating on the atomic scale is speed (figure 5). For example, the minimum switching time t is given by the uncertainty relation $t = h/E$, where E is the switching energy [23]. E has to be larger than the minimum energy $E_{min} = k_B T \ln 2$ for switching one bit [23, 24]. In our case, the activation energy of 1.2 eV for moving one Si atom is much larger than $k_B T = 25$ meV. In principle, that would allow very fast switching and writing.

The readout, however, has to slow down for small bits since the signal decreases and becomes noisier. In our case,
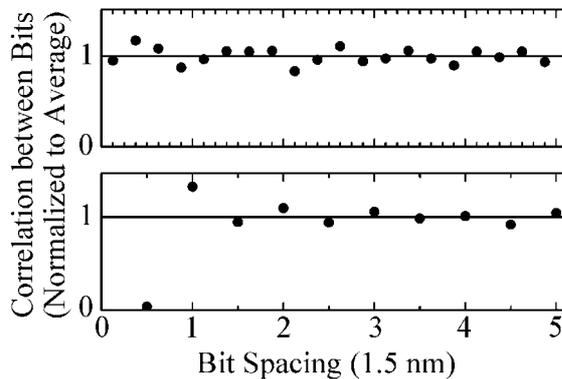
Figure 4. The autocorrelation between neighbouring Si atoms as a test of interactions between adjacent bits. The closest 5×2 site along a track is nearly excluded (bottom), showing that 5×4 atoms form the minimum viable cell. Neighbouring tracks are not correlated (top).
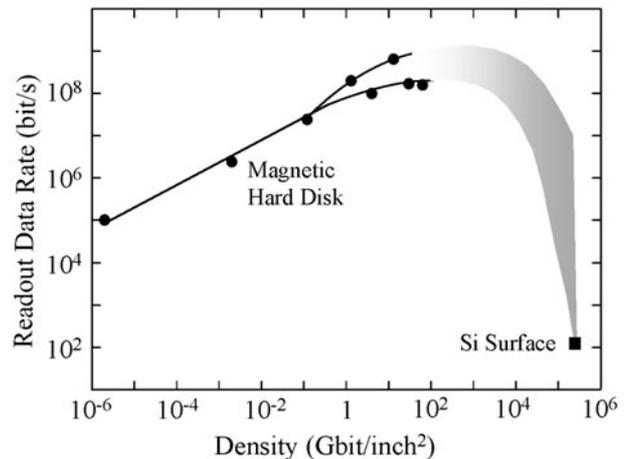
Figure 5. Trade-off between readout speed and storage density at the atomic limit.

501

the tunnelling current is affected by statistical fluctuations in the number of electrons and by thermal noise. Their respective spectral densities are $S_s(\omega) = 2eI$ and $S_t(\omega) = 4k_BT/R$, resulting in current fluctuations of 8 and 1.3 fA Hz$^{-1/2}$ for our conditions ($I = 0.2$ nA, $R = 10^{10}$ Ω, $T = 300$ K). Adding the two noise contributions and integrating over a dwell time of $\tau = 500$ μs/point, one finds a current fluctuation $\delta I = [(S_s+S_t)/\tau]^{1/2} = 3.6 \times 10^{-13}$ A. This current fluctuation is translated into a height fluctuation δz via the exponential dependence $I(z) = I_0 \exp(-kz)$ of the tunnelling current on z:

$$\delta z = \delta I/(\partial I/\partial z) = \delta I/(-kI) = 9 \times 10^{-5} \text{ nm}$$

with $k = 20$ nm^{-1} for a typical tunnel barrier of 4 eV. That is 55 times smaller than the actual noise $\delta z = 0.005$ nm. Statistical and thermal noise would meet this level with a dwell time of only 160 ns (200 electrons/point). The corresponding readout speed would be 6×10^6 points s^{-1}, which is respectable but still slower than today's hard disks (figure 5). High-speed STM amplifiers operating at rates up to 50 MHz exist [25].

A further tool for enhancing speed is a high degree of parallelism (see the discussion in [24] and [26]). In fact, there has been a substantial effort directed at producing large arrays of scanning probe tips by silicon processing methods. An array of $32 \times 32 = 1024$ tips with 92 μm pitch is operational [27]. The atomic precision of the tracks ensures that the tip array follows the tracks after a one-time adjustment of the tip positions and the scan direction.

4. Outlook

An interesting yardstick is the storage and transcription of data in biological systems. $5 \times 4 = 20$ surface atoms store one bit on silicon compared to 32 atoms used by DNA (64 atoms for an AT base pair plus backbone, 63 atoms for CG, with each base pair coding the four combinations AT, TA, CG, GC, i.e. 2 bits). The transcription rate from DNA to RNA is ≈ 60 nucleotides s^{-1} for E-coli at 37 °C and 10 times faster for DNA replication. The STM acquisition rate on silicon is comparable (120 bit s^{-1} in figure 2(e)). It could be as high as 10^7 bit s^{-1} at the statistical noise limit. Parallel readout can be used in both cases, with $\approx 10^1$ subsections of DNA being replicated simultaneously and an array of 10^3 tips scanning in parallel. Cells use a similar parallelism of 10^3–10^4 for protein synthesis, where speed is more important. The error rate achieved in DNA replication is as low as 10^{-7}–10^{-11} with error correction by DNA polymerase.

Compared to conventional storage media, both DNA and the silicon surface excel by their storage density (compare figure 1 for CD-ROM). The highest density achieved in hard-disk demos is about 100 Gbit inch^{-2}, whereas the Si atom memory exhibits 250 Tbit inch^{-2}. However, the push towards the atomic density limit requires a sacrifice in speed, as demonstrated in figure 5. Practical data storage might evolve

in a similar direction, with the gain in speed slows down as the density increases. Somewhere on the way to the atomic scale ought to be an optimum combination of density and speed.

Acknowledgment

References

[1] Tseng G Y and Ellenbogen J C 2001 *Science* **294** 1293
[2] Chen J, Reed M A, Rawlet A M and Tour J M 1999 *Science* **286** 1550
[3] Collier C P, Mattersteig G, Wong E W, Yi Luo, Berverly K, Sampaio J, Raymo F M, Stoddart J F and Heath J R 2000 *Science* **289** 1172
[4] Rueckes T, Kim K, Joselevich E, Tseng G Y, Cheung C L and Lieber C M 2000 *Science* **289** 94
[5] The CD-ROM image is from Digital Instruments: webpage http://www.di.com/movies/movies_inhance/appnotes/odt/odtmain.html
[6] Eigler D M and Schweizer E 1990 *Nature* **344** 524
[7] Whitman L J, Stroscio J A, Dragoset R A and Celotta R J 1991 *Science* **251** 1206
[8] Uchida H, Huang D, Grey F and Aono M 1993 *Phys. Rev. Lett.* **70** 2040
[9] Hosaka S, Hosoki S, Hasegawa T, Koyanagi H, Shintani T and Miyamoto M 1995 *J. Vac. Sci. Technol.* B **13** 2813
[10] Shen T C, Wang C, Abeln G C, Tucker J R, Lyding J W, Avouris Ph and Walkup R E 1995 *Science* **268** 1590
[11] Avouris Ph 1995 *Acc. Chem. Res.* **28** 95
[12] Jung T A, Schlittler R R, Gimzewski J K, Tang H and Joachim C 1996 *Science* **271** 181
[13] Dujardin G, Mayne A, Robert O, Rose F, Joachim C and Tang H 1998 *Phys. Rev. Lett.* **80** 3085
[14] Quaade U J, Stockbro K, Lin R and Grey F 2001 *Nanotechnology* **12** 265
[15] Hasegawa T and Hosoki S 1996 *Phys. Rev.* B **54** 10 300
[16] Yagi Y, Kakitani K and Yoshimori A 1996 *Surf. Sci.* **356** 47
[17] Altmann K N, Crain J N, Kirakosian A, Lin J L, Petrovykh D Y, Himpsel F J and Losio R 2000 *Phys. Rev. Lett.* **85** 808
Altmann K N *et al* 2001 *Phys. Rev.* B **64** 035406
[18] Bertram H N, Zhou H and Gustafson R 1998 *IEEE Trans. Magn.* **34** 1845
[19] Tsang C *et al* 1999 *IEEE Trans. Magn.* **35** 689
Schultz M A, Malhotra S S, Lal B B, Kimmal J M, Russak M A, Liu F, Stoev K, Shi S, Hua Ching Tong and Dey S 2000 *IEEE Trans. Magn.* **36** 2143
[20] Wood R 2000 *IEEE Trans. Magn.* **36** 36
[21] Cowburn R P and Welland M E 2000 *Science* **287** 1466
[22] Kubetzka A, Piezsch O, Bode M and Wiesendanger R 2001 *Phys. Rev.* B **63** 140407
[23] Meindl J D, Chen Q C and Davis J A 2001 *Science* **293** 2044
[24] Williams R S 1998 *Phil. Trans. R. Soc.* A **356** 1783
[25] Jersch J, Demming F, Fedotov I and Dickmann K 1999 *Rev. Sci. Instrum.* **70** 3173
[26] Rohrer H 1998 *Microelectron. Eng.* **41–2** 31
[27] Vettiger P, Despont M, Drechsler U, Durig U, Haberle W, Lutwyche M I, Rothuizen H E, Stutz R, Widmer R and Binnig G K 2000 *IBM J. Res. Dev.* **44** 323