Physics 623

A Phase Locked Loop

In this lab we will use a popular 16 pin package MC14046 which contains a Voltage Controlled Oscillator (VCO) and two types of phase comparators. In addition there is a high impedance Source Follower (SF) which allows one to monitor the input to the VCO without disturbing the action of any preceding filter with excessive loading.

The chip is CMOS. Although higher voltages are possible as detailed by the specification sheet, we will operate our chip from a +5 Volt supply and be careful to maintain TTL logic levels (0-5V) at the input. Make certain the D.C. offset on the Wavetek is set at zero Volts.

The sensitive FET gates are adequately protected so that you should not need to observe such precautions as a ground strap on your wrist to avoid static discharge. It would be a good idea not to apply input signals when there is no DC power on the chip, however this chip is probably rugged enough not to be degraded by such treatment.

Connect your chip in a standard Phase Lock Loop configuration as shown in figure 1. Initially use the XOR comparator output from pin 2. In a Phase Lock Loop the A.C. output of the comparator is always fed into a filter to provide a D.C. control voltage for the the VCO. The output of the VCO is then returned to the comparator to be matched against the input from the Wavetek. In general one has to be careful to get the polarity of feedback correct, but in this case there is only one possible connection.

Run the Wavetek in the CONTINUOUS Mode. Use a square wave at about 1 kHz, oscillating between 0V and +5V. Trigger the scope with the input Wavetek signal. (At frequencies this low it may seem more advantageous to view the second scope channel with the CHOPPED rather than the ALTERNATE mode on scopes using these features.)

Vary the Wavetek frequency over a wide range and observe how the VCO will sometimes lock in synchronization with the Wavetek and sometimes run freely out of phase. Notice that in the locked condition there is a stable voltage input to the VCO as read by a digital voltmeter at the SF output.

First distinguish qualitatively between the lock-in range of frequency and

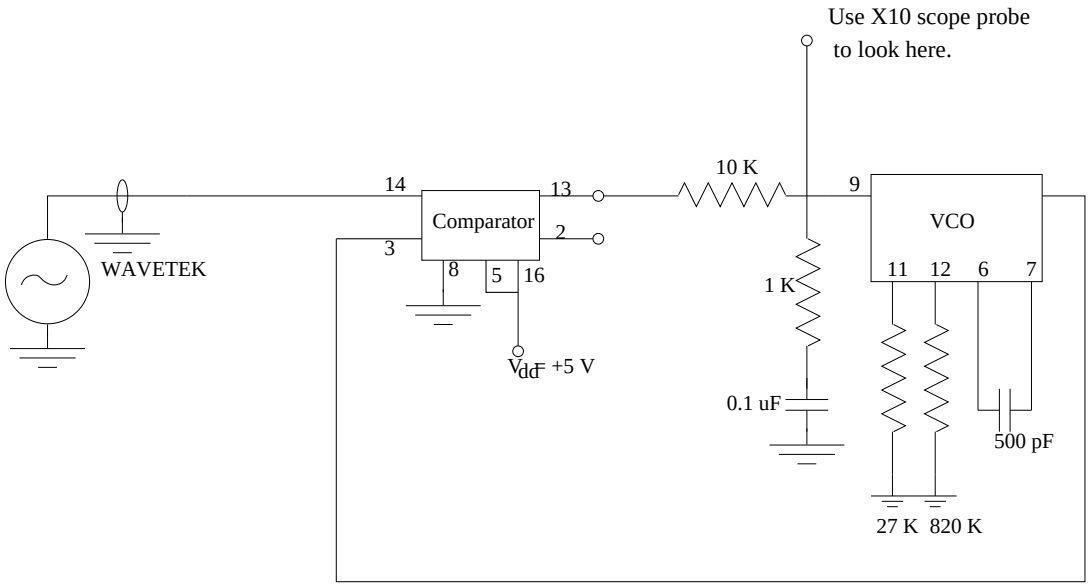

Figure 1:

the capture range of frequency. The lock-in range is usually greater than the capture range. Once locked in, the input frequency can be moved slowly over a wide range and the VCO will stay locked in phase. However, once the locked condition is lost, the input frequency may need to be adjusted to recapture the locked condition.

Make a note of the high and low frequencies of your lock-in range and the D.C. level of the input to the VCO at these limits. Vary the Wavetek frequency so as to approach the lock-in range from outside the range, and try to find similar high and low limits for lock-in capture. While the VCO is locked in, plot the VCO input DC level for several frequencies and comment on the linearity of the DC level as a function of frequency.

While still using the XOR output of the comparator (pin 2), vary the Wavetek frequency over the lock-in range and observe how the relative phase between the VCO and Wavetek depends on frequency. Explain why this phase variation is necessary if the XOR comparator is to influence the frequency of the VCO.

Note there are frequencies outside of the normal lock range where the VCO and Wavetek will lock in phase, but where the two oscillator frequencies

have a harmonic relationship to each other. Locate at least one of these and measure the frequency ratio of the two oscillators.

Switch from the XOR comparator output to the alternative comparator output from pin 13. This alternative comparator has a set of gates arranged to sense several pairs of information about the pulse edges of the VCO and Wavetek pulses.

The alternative comparator logic is such that it charges an output capacitor for any amount of time that the Wavetek is on before the VCO and discharges the capacitor for any amount of time the VCO is on before the Wavetek. Because of the edge sensing, this comparator does not react to harmonic relationships between the two oscillators as the XOR comparator does.

Find the lock-in and capture frequency range for this new comparator. Convince yourself that it does not lock in on harmonics. Check to see if the phase varies between the Wavetek and VCO as the frequency is varied over the lock range.

An obvious application of the PLL we have set up here is a frequency-to-voltage conversion. This could be used as a demodulator for a signal that is frequency modulated (FM detector). The modulation frequency would have to be low enough to be passed by the filter.

Another application of the PLL is frequency multiplication. A highly stable and precise frequency source (represented by our Wavetek) can be multiplied to a precise high frequency. A specific case would be to multiply 30 Hz (frames/sec) by 525 (lines/frame) to produce a trigger for 15,750 horizontal sweep lines per second on a television screen. Or a single crystal oscillator could be multiplied by integers that would step an FM detector through the stations on a radio dial.

To illustrate frequency multiplication, we insert a 4-bit synchronous counter (74LS193) in the feedback loop as sketched in figure 2. Continue to use the alternative comparator output from pin 13. Add two 1 μF capacitors in parallel to the filter. The added capacitance will slow the response time of the PLL to frequency variations, but it will also be less sensitive to short term noise, which is desirable in this application.

Begin by extracting the counter output from pin 6 in order to divide by 8X. Set the Wavetek at 90 or 100 Hz and search for lock-in by comparing the VCO output at pin 4 to the Wavetek output. Use the Wavetek to trigger the scope and expand the scope sweep until you get a good measure of the

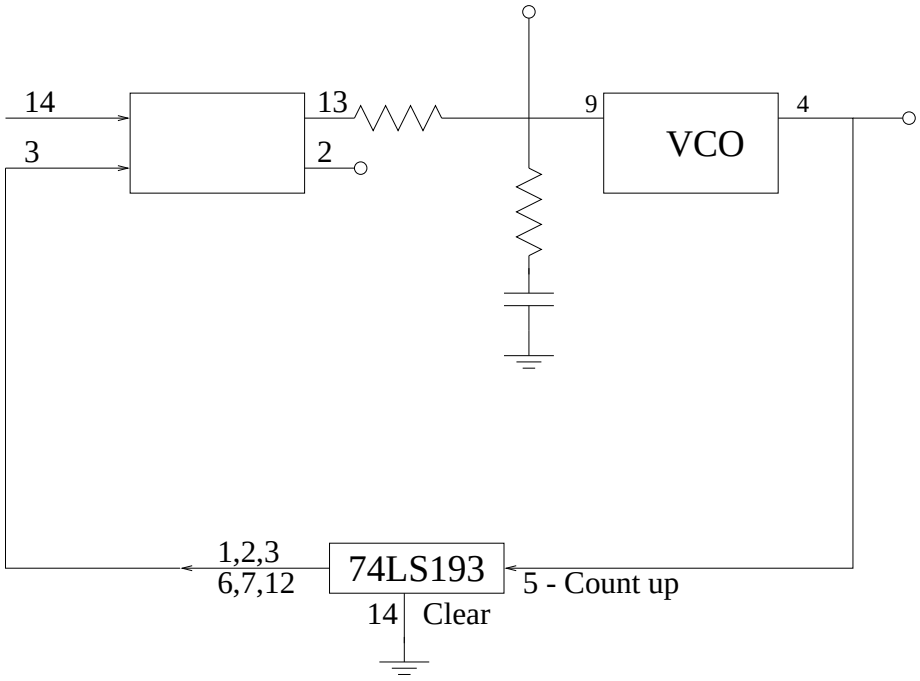

Figure 2:

time jitter between the Wavetek and the VCO outputs. Remove one of the 1 μF capacitors and see if you can measure a change in this jitter. If you have time, you might want to try scaling also by 2, 4, or 8.

With some care it is possible for us to observe the classic transient behavior of the PLL as it locks on to a signal. Set up the HP pulser to gate on the Wavetek automatically as follows. Run the pulser with a period of about 5 seconds and pulse width of about 0.2 seconds. Amplitude $\sim$ 5 V. Set the Wavetek Mode switch to "Gated" and drive the "Trig In" BNC connector of the Wavetek with a positive output from the HP puler. Use the center knob of the MODE switch to adjust the Wavetek discriminator level downward until the Wavetek puts out 0.2 second long bursts of output pulses.

Trigger Channel 1 of the scope with the Wavetek output and observe the filter output (SF) on Channel 2 during the 200 msec of the Wavetek burst. You should be able to see the asymptotic approach to lock-in on Channel 2. Try 1 μF and 2 μF in the filter. Compare scaling by 8X with no scaling.