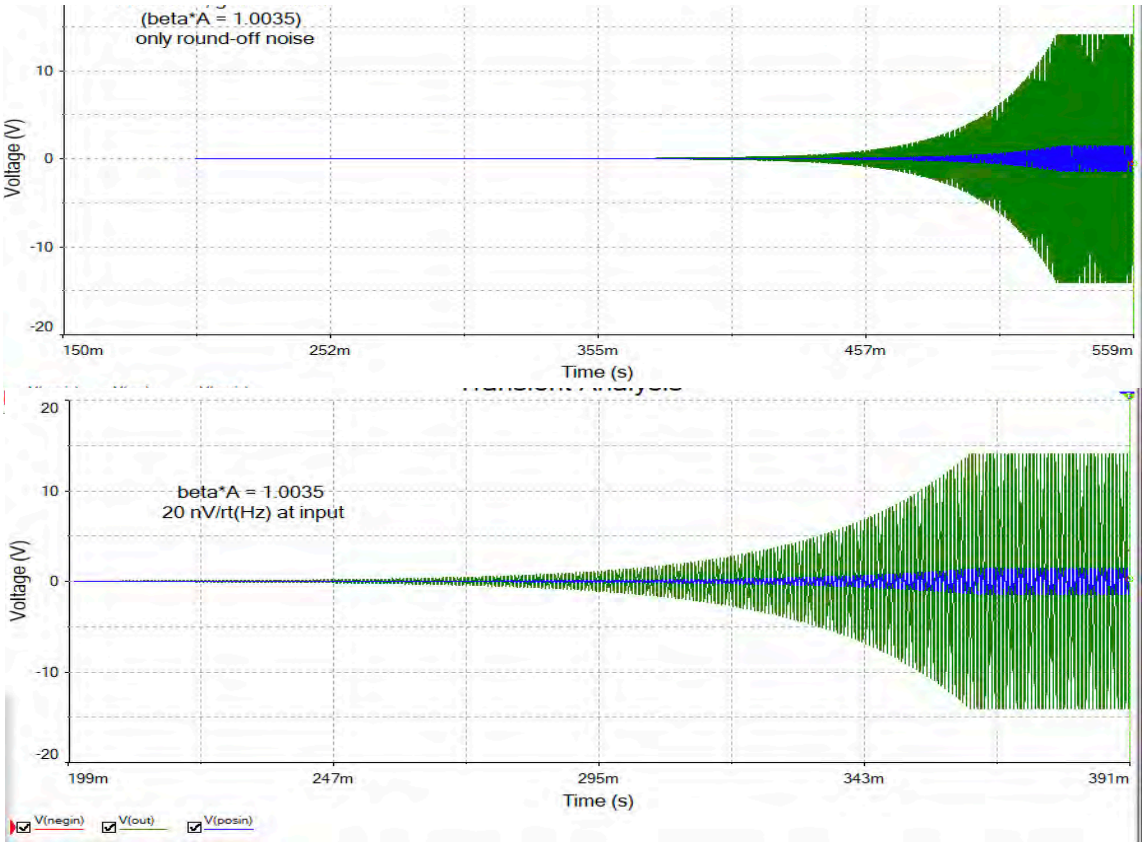
Oscillator Lab — Supplement for Remote Version

The lab instructions from the course website are still the primary guide for the experiment. You should simulate the four circuits shown in Figures 1-4, examine the results, explain what you see, and compare them with your expectations.

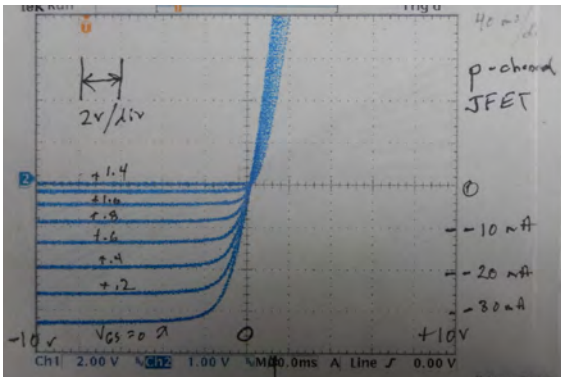
For the circuit in Figure 3, you can vary the gain A by changing the adjustable resistor. You should experiment with this to see what minimum gain is required, and whether this is consistent with your calculation of the magnitude of β at the frequency where it is positive real. You can see the distortion of the saturated waveform, and test whether you can adjust A close enough to the critical value to keep it from saturating, as it suggests in the experiment instructions. The adjustments to the variable resistor can be made as fine as you like, but don't waste a lot of time on this, since you have to run a whole new simulation for each setting. It was much easier in the real lab where you could just watch the scope while you adjusted the resistor.

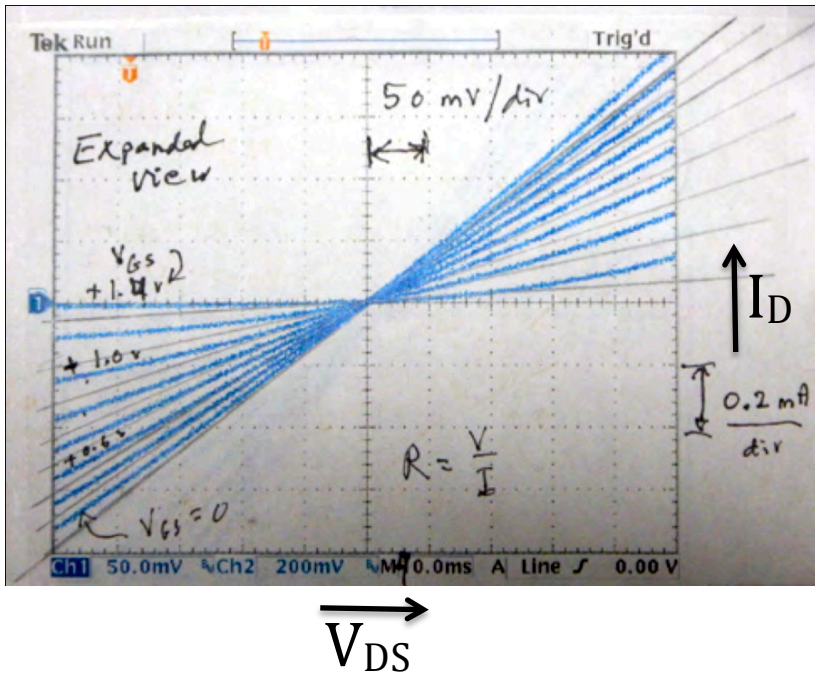
The other thing that slows you down is that when you're close to the minimum A ($\beta A = 1 + \varepsilon$), it takes a long time for the oscillator to start up. The Multisim model for the 741 apparently doesn't have any noise included, so you have to get your starting signal from round-off errors in the calculation. Since multisim does everything in double-precision, you're really starting small. I tried adding a 20 nV/rt(Hz) voltage source, comparable to the specified 741 noise, in series with the op-amp input (remember our equivalent circuit for a real op amp with a noise-free ideal amp and external noise sources?), and it gets going quite a bit faster (note that time axes don't start at zero and are not the same):



For the circuit in Figure 4, note that the gain A of the amplifier is determined by the voltage divider consisting of the adjustable resistor (maximum value 10 k), and the FET channel. If you are successful and the circuit oscillates with a stable amplitude that is not saturated, you know that βA is exactly one. You calculated the magnitude of β at the frequency where it is positive real, so you know what A must be. So for any setting of the adjustable resistor, you can calculate the resistance of the FET.

You don't have access to the curve tracer in the lab, so here are screen shots from a 2N4360 p-channel JFET that I measured:





The left picture shows the normal p-channel FET curves in the lower left quadrant. The picture on the right shows a much-expanded view of the "triode" or linear region, where V_{DS}, the voltage drop along the channel, is very small compared to the pinch-off voltage (≈ V_{GS} where I_D goes to zero). So in this region, the voltage between the gate and the channel remains close to V_{GS} along the entire length of the channel, and the resistance of the channel is independent of I_D and its direction (since the construction of the FET is symmetrical, the difference between source and drain is defined only by the sign of the voltage drop along the channel, so as long as this is negligible, it shouldn't matter which way the current is going).

Given your calculation of the magnitude of β when it is positive real, calculate the value of the channel resistance for βA = 1 if the adjustable resistor is set to 75% (7.5 k ohms). Using the data above, estimate the value of V_{GS} required to achieve this resistance for this particular FET. Show this calculation in your lab report.

Multisim does not have a model for the 2N4360 nor the NTE326. The 2N2608 seems to have similar characteristics, with a somewhat lower pinch-off voltage, so I suggest you use that.

Note from the curves above that the channel resistance becomes nonlinear if V_{DS} exceeds 100 mV or so, particularly on the positive side. The peak voltage across the FET is just the voltage divider ratio, or βV_{OUT}, so you would like to keep the peak value of V_{OUT} below $0.1V/\beta$. Since the 0.1 μF capacitor charges to close to the peak value of V_{OUT}, you want to keep V_{GS} below $0.1\ V/\beta$ as well. This gives you a maximum value for the adjustable resistor. Of course, your FET will be different, so you'll have to experiment and see how the output amplitude depends on the adjustable resistor setting, and how the distortion depends on the amplitude.