Ph 623 - 14 April

Labs - Can't get PLL working reasonably
Is simulation of D/A - A/D lab worthwhile
Alternative is 3 FPGA labs

Try to get simulation lab done by end of week.
Send me questions

H+H P.I.D. controller for temperature 15.6.2

S.A.R. in A/D : 13.7

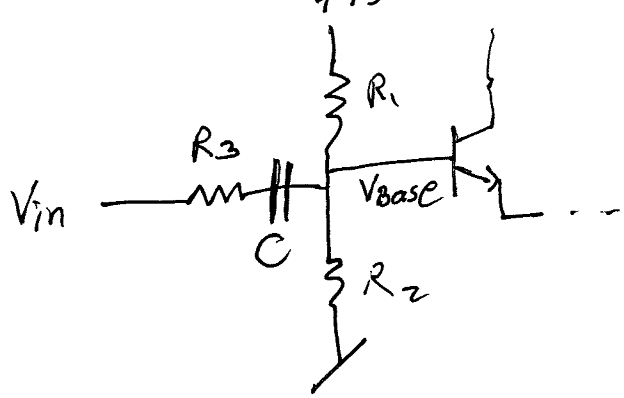
Dual Slope (integrating) A/D : 13.84

Σ-Δ ADC 13.9 ffff ← Good explanation, but requires considerable time investment - won't get much out of skimming.

Mathematician's Approach:

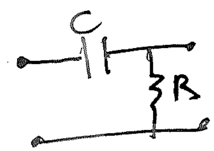
– reduce it to a problem you've Solved before

Something you'll need for sim. lab



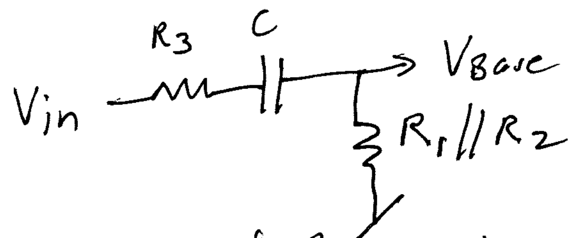
What is $\frac{V_{base}}{V_{in}}(\omega)$

You Know:

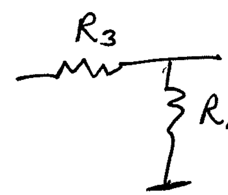


$= \frac{R}{R+\frac{1}{i\omega C}} = \frac{i\omega RC}{1+i\omega RC}$

~~Small~~ A.C. problem, so $+15 = GND$



Hi-F limit:



$\frac{V_B}{V_{in}} \rightarrow \frac{R_{\|}}{R_3+R_{\|}}$

Capacitor has to charge thru both resistors in series, so expect $\tau = (R_3+R_{\|})C$.

$\therefore$ Expect $\frac{V_{Base}}{V_{in}} = \frac{R_{\|}}{R_3+R_{\|}} \cdot \frac{i\omega(R_3+R_{\|})C}{1+i\omega(R_3+R_{\|})C}$

So lower corner should be at

$$\omega = \frac{1}{(R_3+R_1\|R_2)C}$$

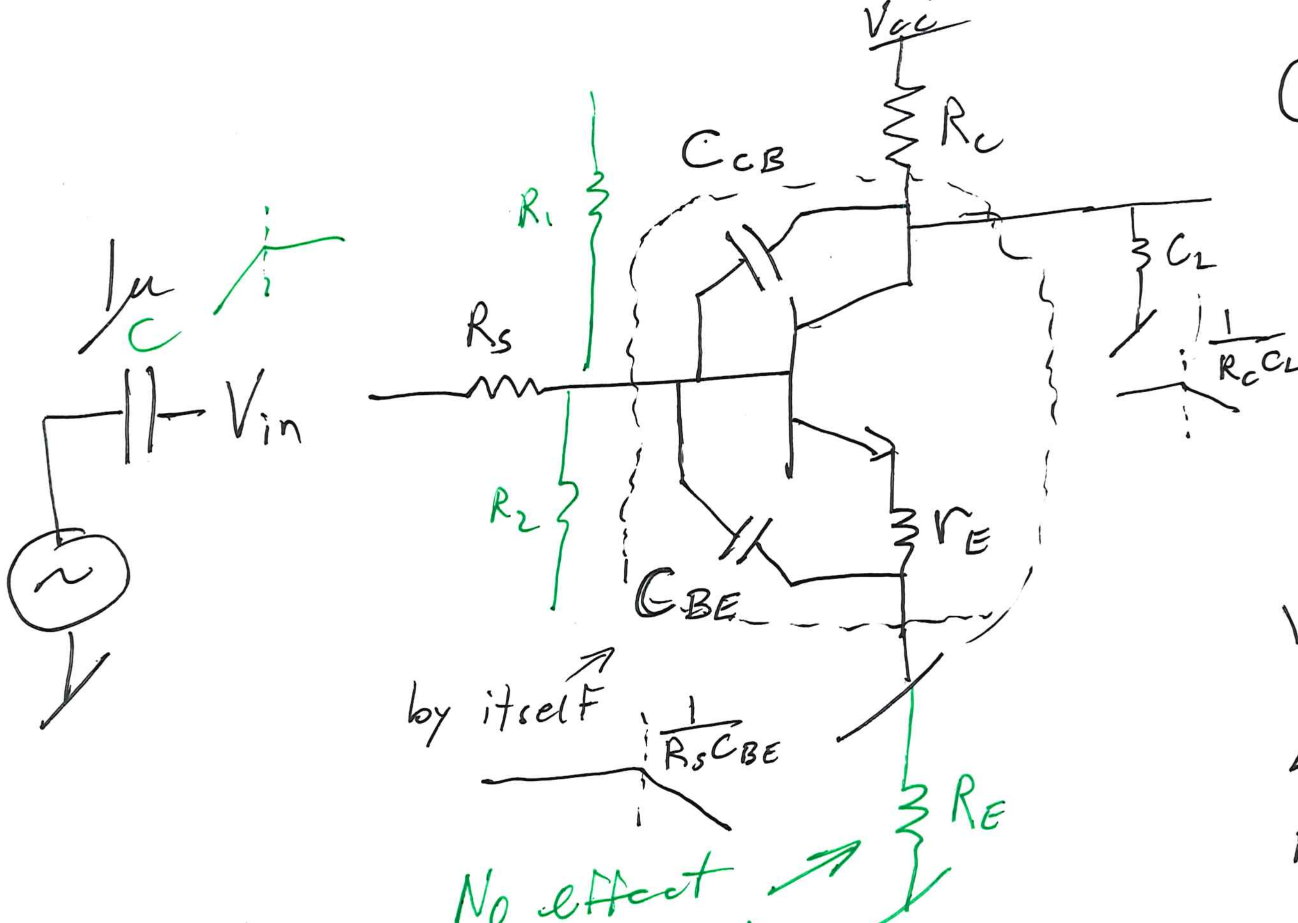
Voltage Divider Eq:

$$\frac{V_B}{V_{in}} = \frac{R_{\|}}{R_{\|}+R_3+\frac{1}{i\omega C}} = \frac{i\omega C R_{\|}}{1+i\omega C(R_{\|}+R_3)}$$

$$= \frac{i\omega C \cancel{R_{\|}} \frac{(R_{\|}+R_3)}{\cancel{R_3}}}{1+i\omega C(R_{\|}+R_3)} \cdot \frac{R_{\|}}{R_{\|}+R_3}$$

Miller Effect: 2.4.5

Will investigate in analog simulation of the differential amplifier you built



No effect of C_{BE} if $\gg r_E$

"Bootstrap"

C_{CB} is bigger problem: gain $A = \frac{-R_c}{r_E (+R_E)}$

$\gg 1$

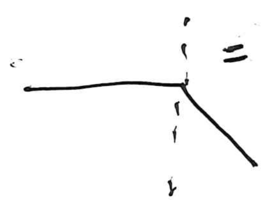
$V_B \uparrow$ by ΔV

$V_c \downarrow$ by $A \Delta V$

$V_{CCB} \uparrow (A+1) \Delta V$

$\Delta Q_{CCB} = (A+1) C_{CB} \Delta V$

From Base looks like $(A+1) \times$ bigger



$= \frac{1}{R_s (A+1) C_{CB}}$

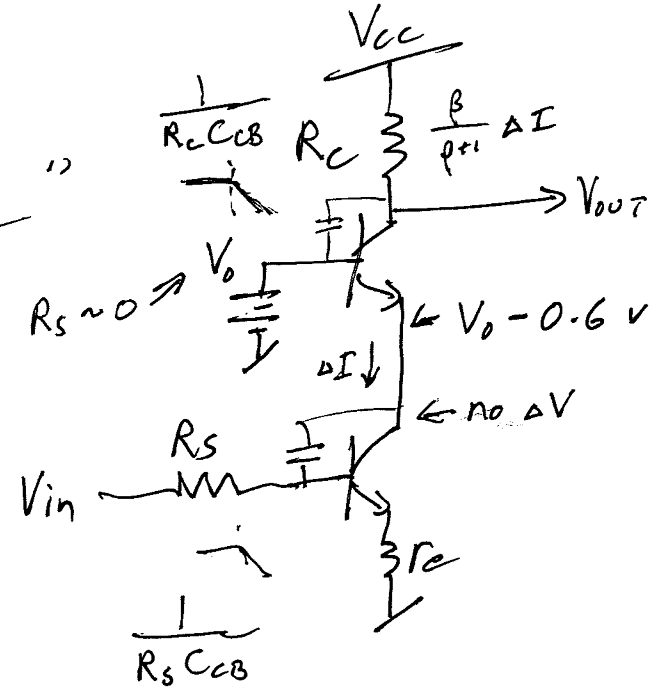
You will investigate this behavior of differential amplifier in sim lab: run with $R_S = 0$ and $R_s = 1K$. High-frequency behavior quite different. See if you can predict upper corner F for $R_S = 1K$

(Model for 2N3904 has $C_{CB} = 3.6\,pF$ – you can edit!)

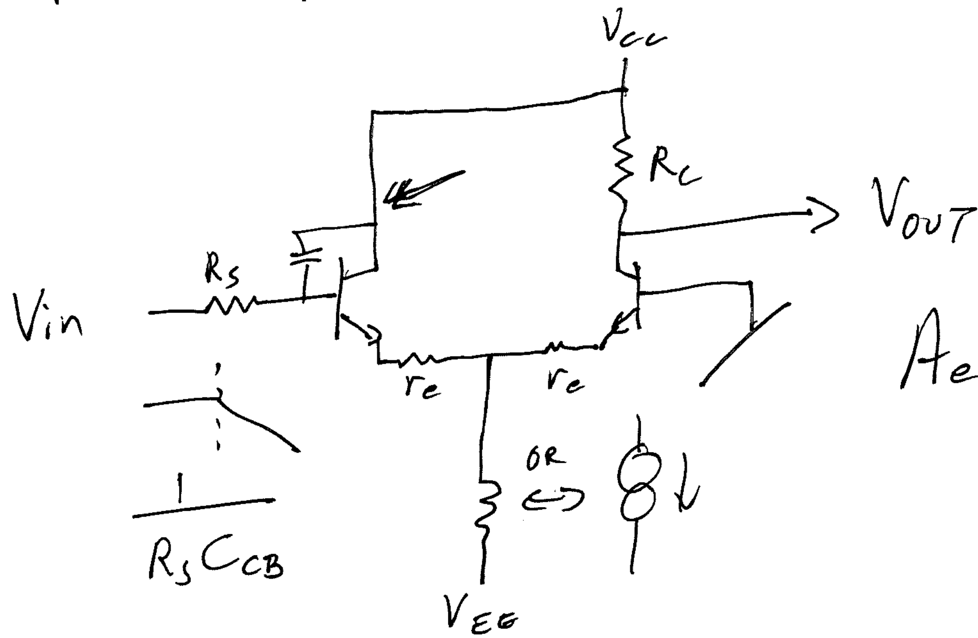
This is big problem for high-freq amplifiers.

Fixes:

"Cascode"



#2 Diff amp



$$\frac{1}{R_s C_{CB}}$$

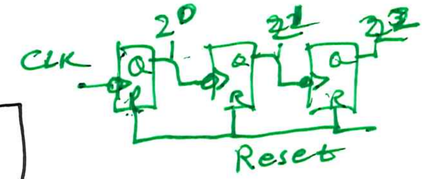
$$V_{Diff} = V_{in} - 0$$

$$V_{cm} = \frac{V_{in} + 0}{2}$$

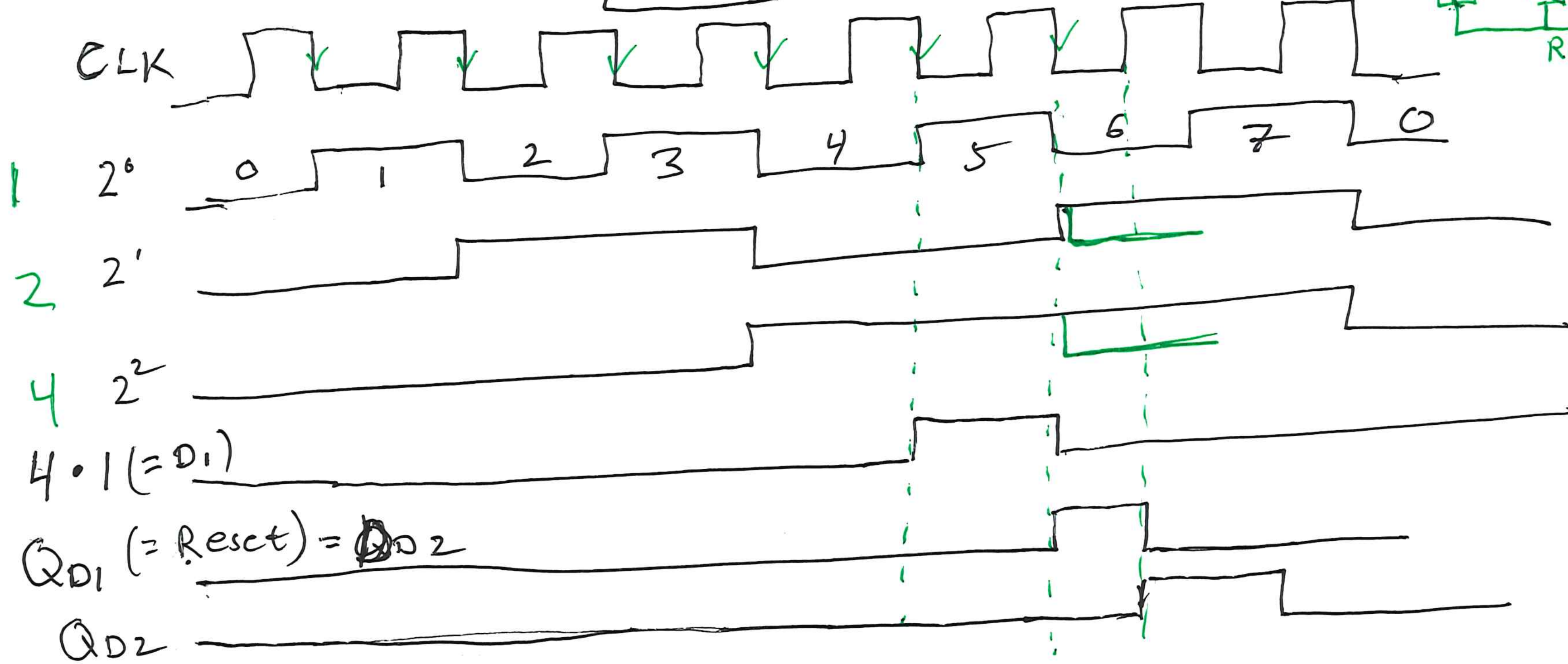
$$A_{eff} = A_{DM} - \frac{1}{2}|A_{cm}|$$

$$A_{cm} \ll A_{DM}$$

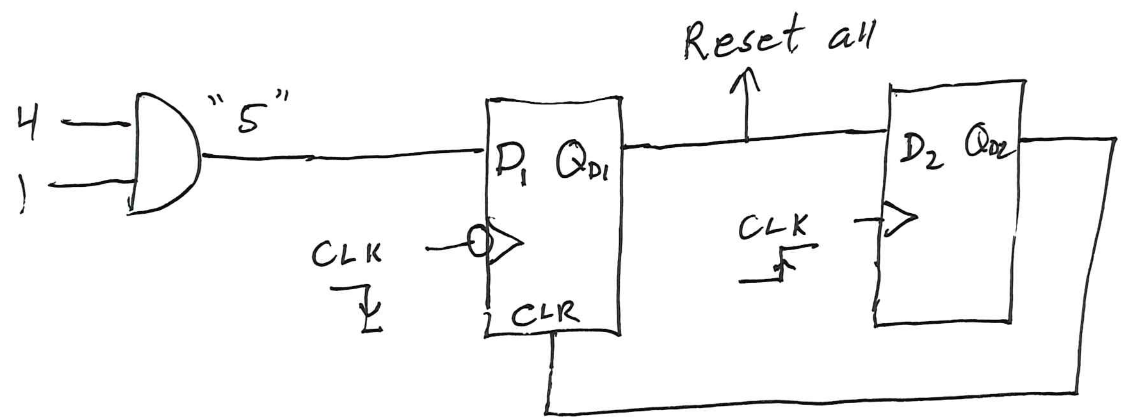
$\boxed{\div 6}$



CLK
2⁰
2¹
2²
Q
R
Reset

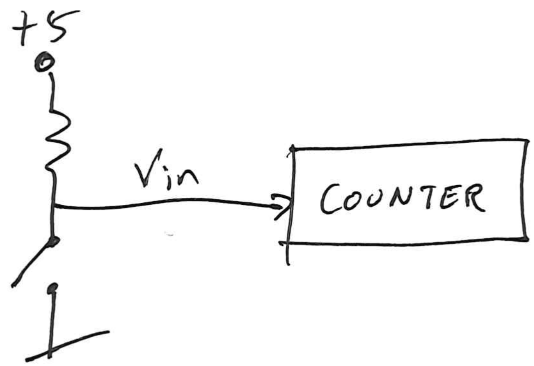


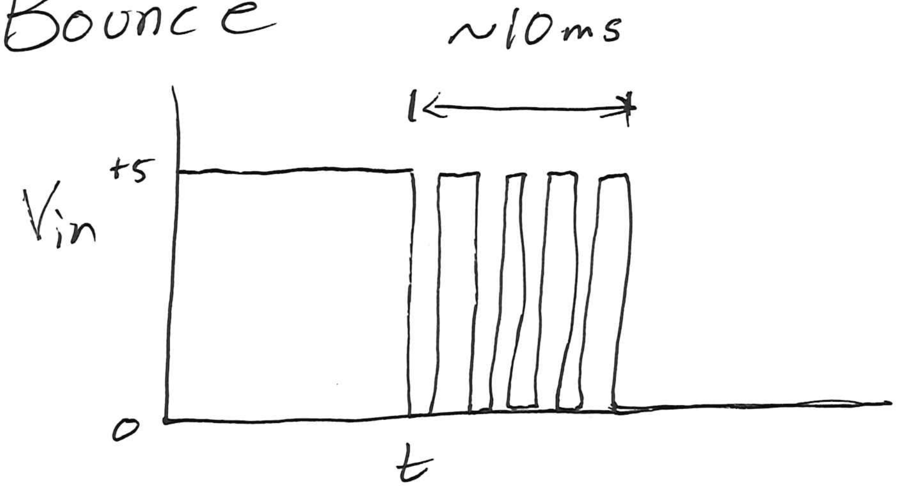
CLK
0
1
2
3
4
5
6
7
0
1 2⁰
2 2¹
4 2²
4•1 (=D1)
QD1 (= Reset) = QD2
QD2



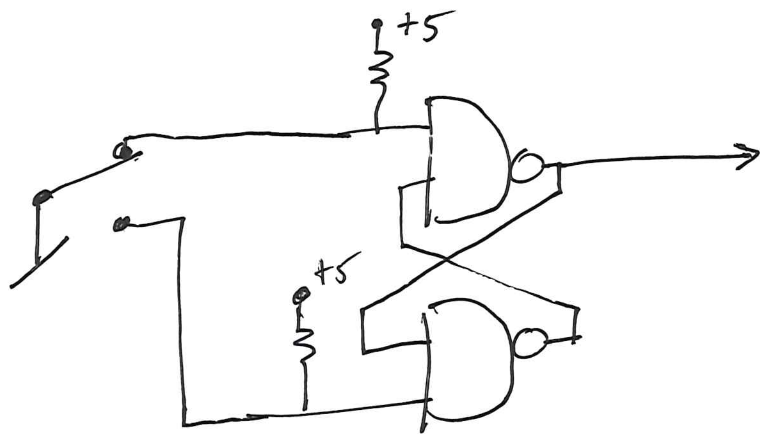
Reset all
4
1
"5"
D1 QD1
CLK
CLR
D2 QD2
CLK

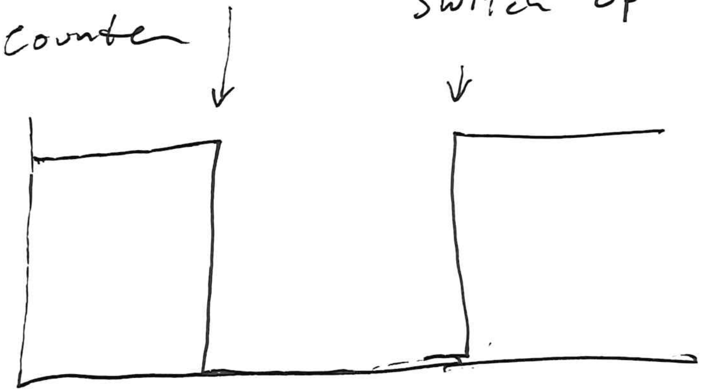
"Switch Bounce"



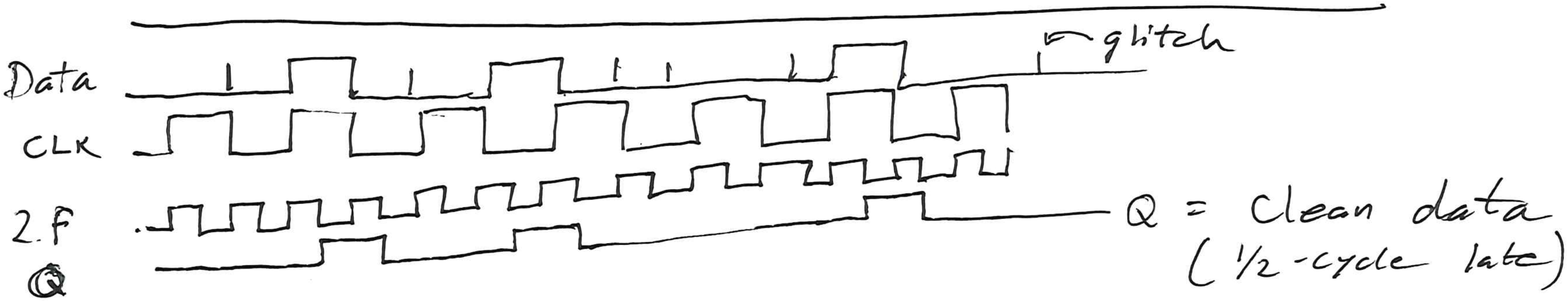


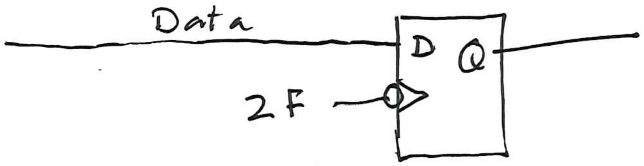
"De-Bounce"



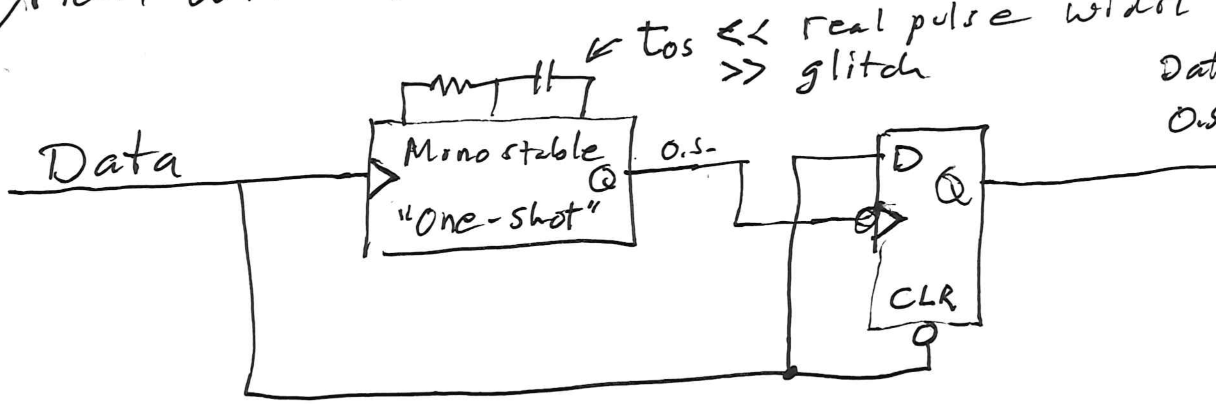


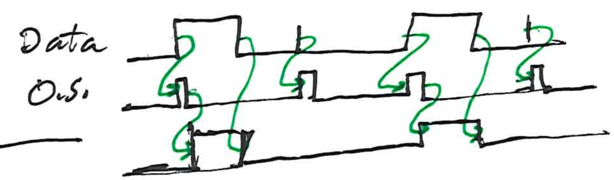
"Glitches"



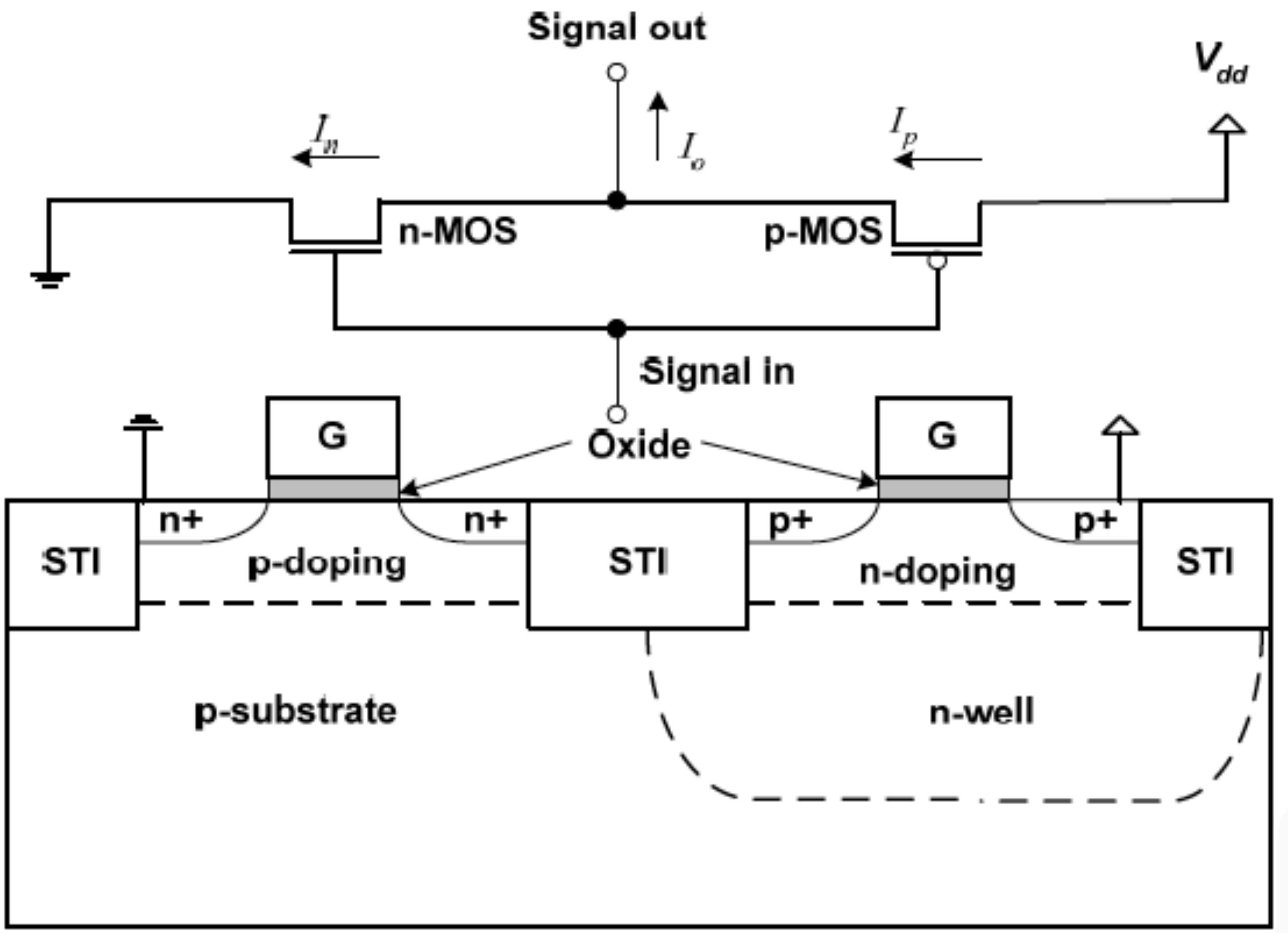


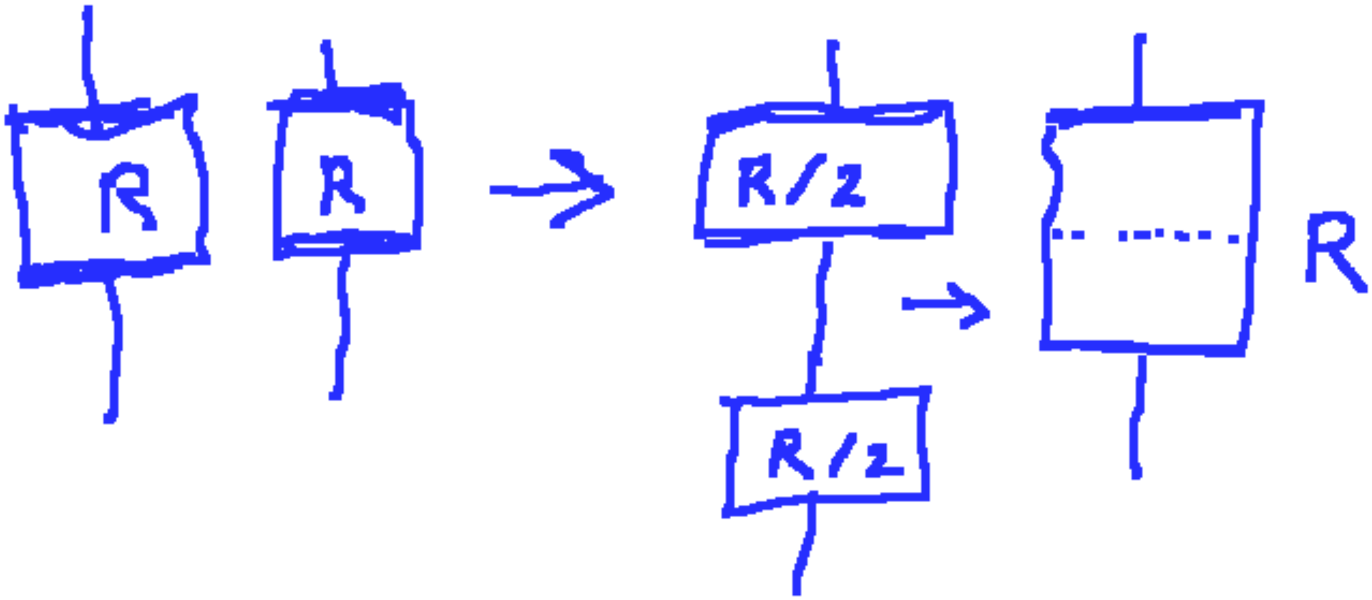
IF data not synchronous (comes from system with different clock:





CMOS Scaling — Origin of Moore's Law





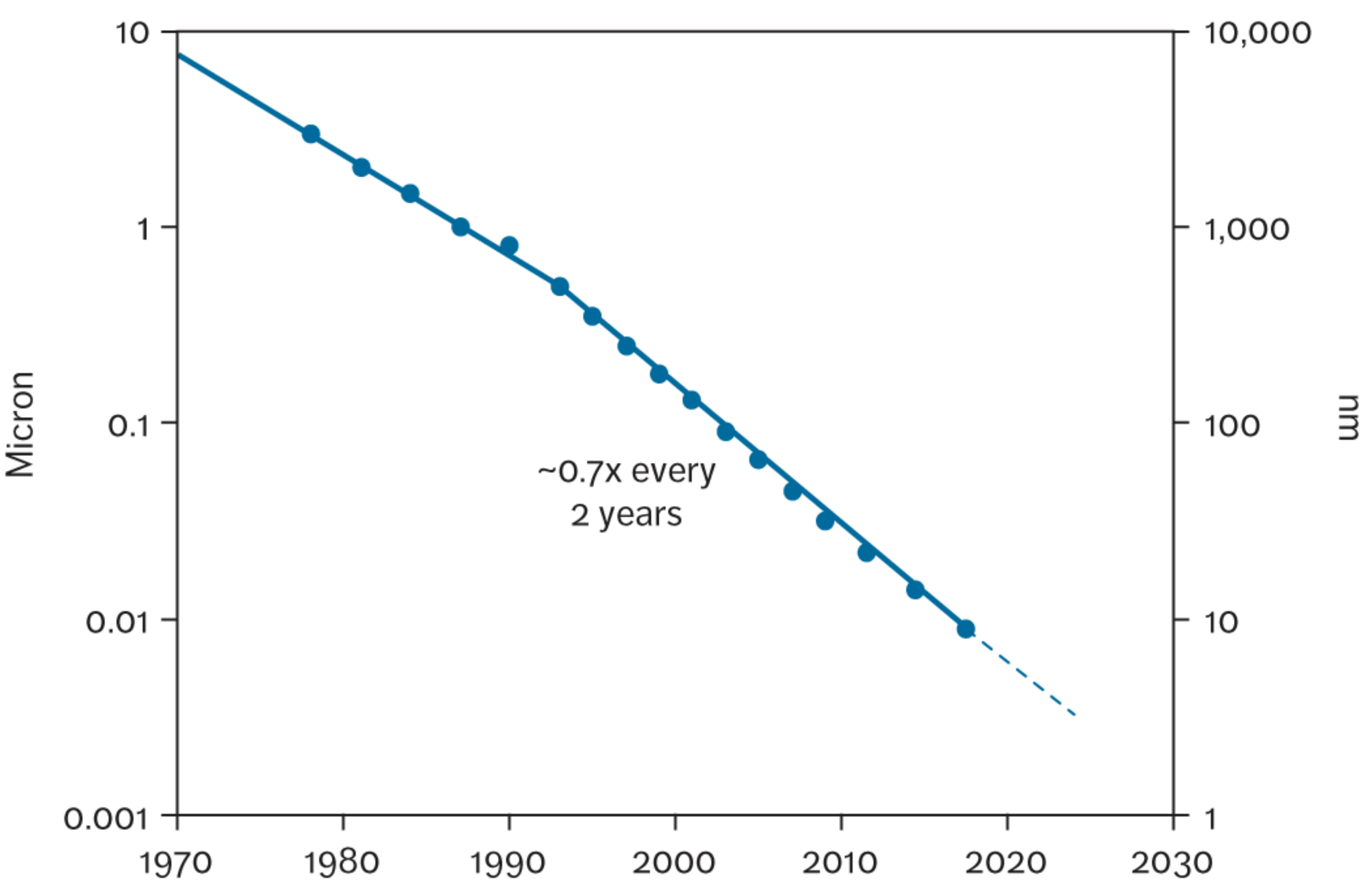
"Sheet Resistance" = "ohms/square"
(independent of size of square)

$$C_{gate} \sim A/d \sim L^2$$

$$\tau \sim RC \;\Rightarrow\; \text{speed} \sim 1/L^2$$

(since R is indep of L)

Devices/Area $\sim 1/L^2$



10
1
0.1
0.01
0.001
Micron
10,000
1,000
100
10
1
nm
1970
1980
1990
2000
2010
2020
2030
~0.7x every
2 years

Problem:

Energy of transition = ½ CV^2

Power ~ $CV^2 f_{\mathrm{max}}$ ~ $L^2\ V^2\ (1/L^2)$ ~ V^2

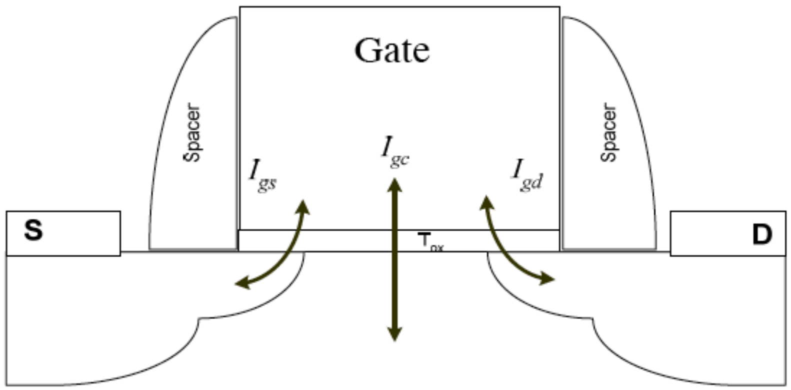
But: Device density ~ $1/L^2$

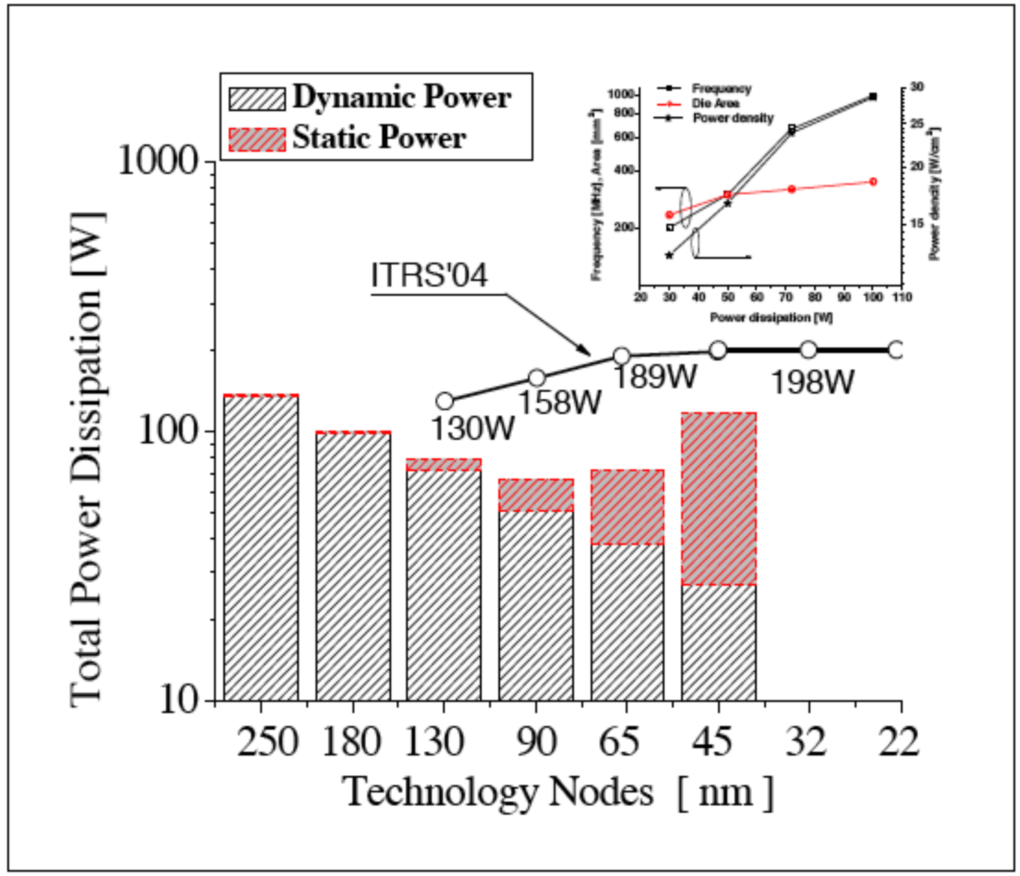
$\Rightarrow$ power density ~ V^2/L^2

So need to reduce V :

5 V → 3.3 V → 2.2 V → 1.8 V → 1.2 V → 0.8 V

Requires thinner oxide


Gate
Spacer
Spacer
I_{gs}
I_{gc}
I_{gd}
S
D
T_{ox}


Dynamic Power
Static Power
ITRS'04
130W
158W
189W
198W
Total Power Dissipation [W]
1000
100
10
250
180
130
90
65
45
32
22
Technology Nodes [nm]
Frequency
Die Area
Power density
Power dissipation [W]