Ph 623
Tue Mar 24

- HW 7 due (email to Joelle
- Oscillator prelab due tomorrow. Lab is due the following Wed.
- Midterm II a week from Thursday

Today:
1. A Few more number systems
2. Parallel Logic (Everything That can be described by a truth table)

Decimal$_{10}$ 12,462 5

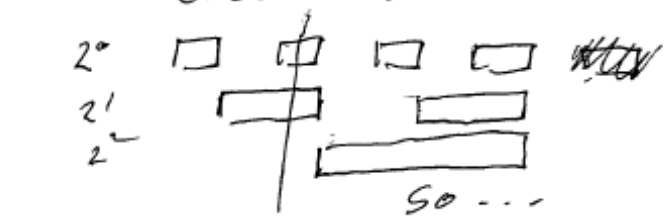
Binary$_2$ 11 0000 1010 1110 14

Octal 8

Hex 16

0-9, A, B, C, D, E, F

Gray Code (usually For mechanical/optical encoders)



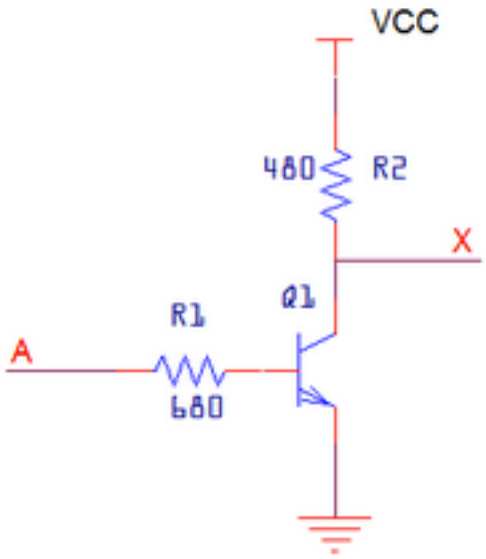
So...

000

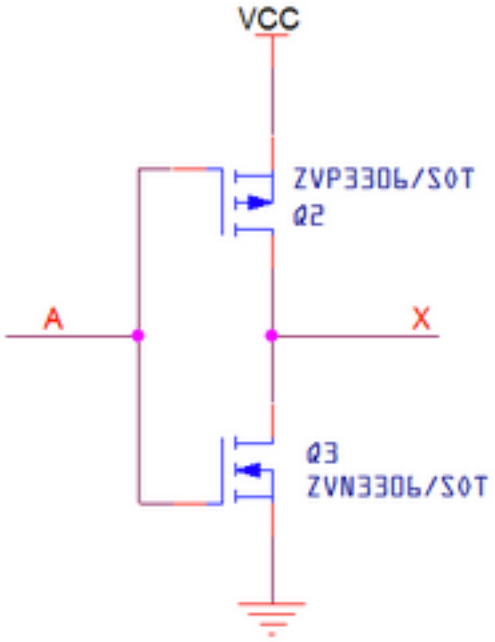
ONLY CHANGE ONE BIT AT EACH Transition

A

Logic “Families”



“TTL”
transistor-transistor logic



“CMOS”
complementary metal-oxide-semiconductor

nomenclature: 74LS157

NAND $X = \overline{A \cdot B}$

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

7400 Quad 2-input
7401 Quad 2-input, open collector outputs
7410 Triple 3-input
7420 Dual 4-input
7430 Single 8-input

NOR $X = \overline{A + B}$

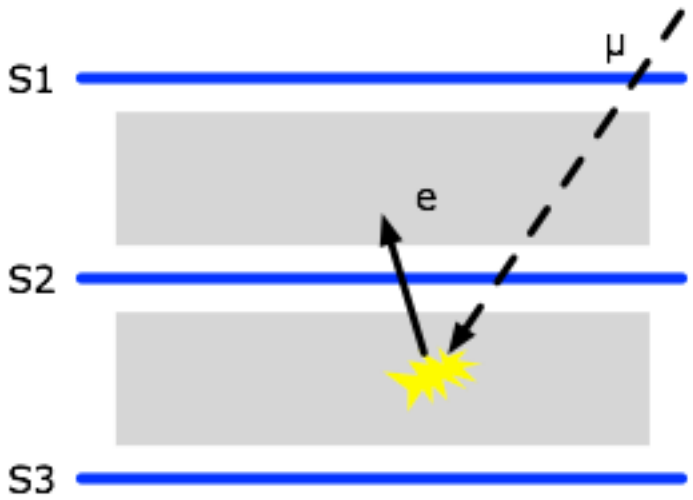
A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

7402 Quad 2-input
7427 Triple 3-input
7425 Dual 4-input

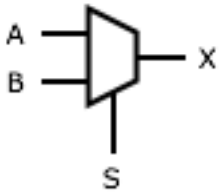
XNOR $X = \overline{A \oplus B}$

A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

74266 Quad 2-input


μ
S1
e
S2
S3

Circuit Symbol



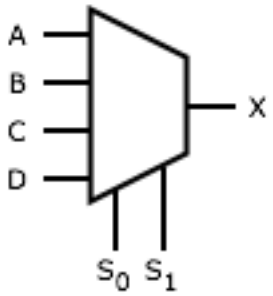
Truth Table

A	B	S	X
0	X	0	0
1	X	0	1
X	0	1	0
X	1	1	1

Description

2-input multiplexer

"Data Selector"



A	B	C	D	S_1	S_0	X
0	X	X	X	0	0	0
1	X	X	X	0	0	1
X	0	X	X	0	1	0
X	1	X	X	0	1	1
X	X	0	X	1	0	0
X	X	1	X	1	0	1
X	X	X	1	1	1	0
X	X	X	1	1	1	1

4-input multiplexer

```
 1 1 1 1   Cy
   1011A
+  0111B
-------
  10010
```

Cin	A	B	X	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

General Scheme for any truth table:

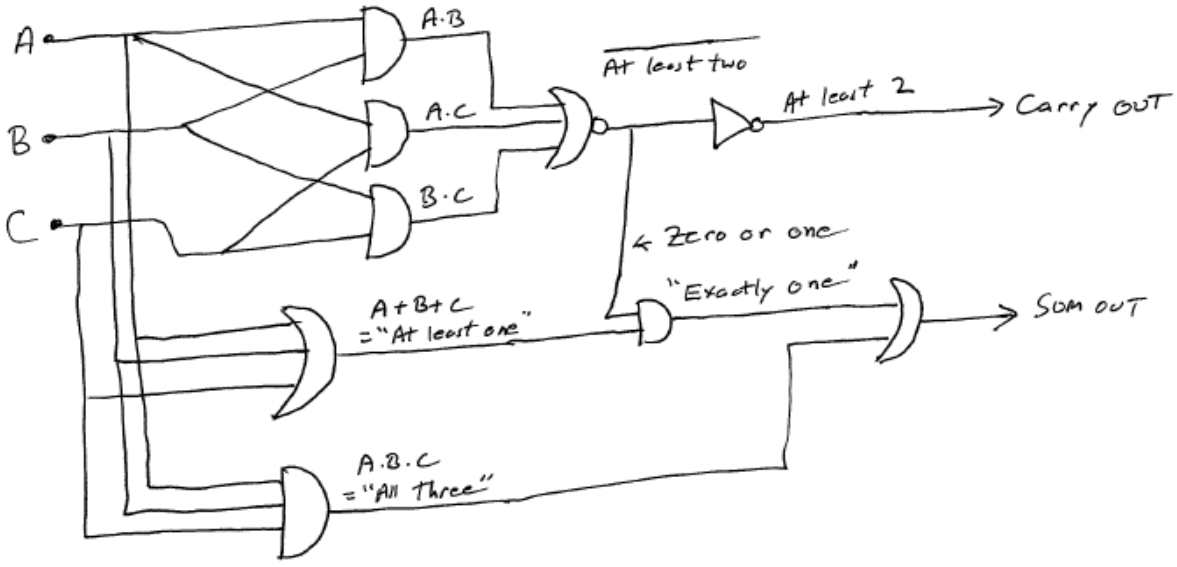
n inputs (n=3)

m outputs (m=2)

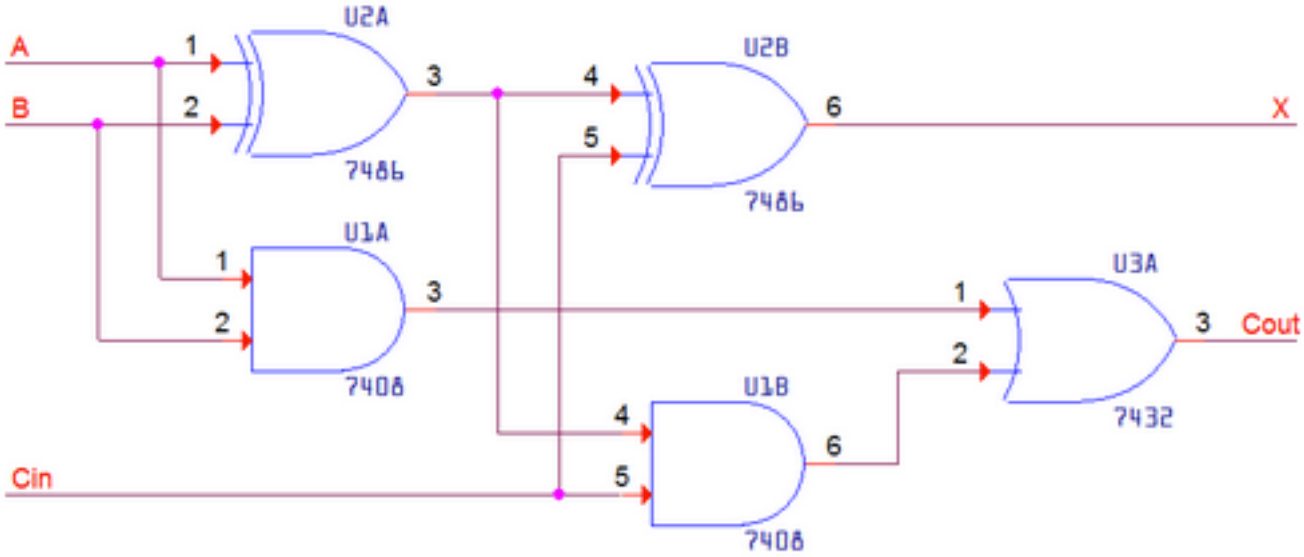
need n inverters to make NOT of inputs

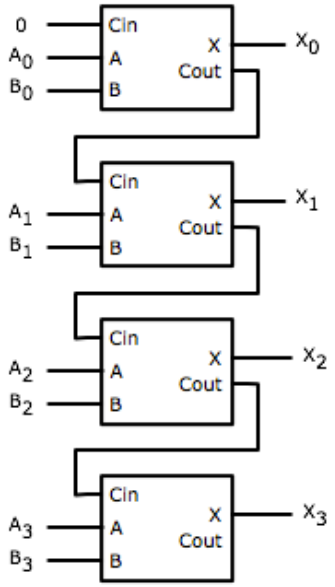
need 2^n n-input AND gates to identify each of the 2^n rows

need m OR gates to generate the outputs with at most 2^n inputs, one input for each '1' in the output column.



C


A
B
Cin
U2A
7486
U2B
7486
U1A
7408
U1B
7408
U3A
7432
X
Cout


0
A0
B0
A1
B1
A2
B2
A3
B3
Cin
A
B
X
Cout
X0
X1
X2
X3