

# Physics 623

## The Difference Amplifier

Sept. 30, 2015

### 1 Purpose

- To construct a difference amplifier, to measure the DC quiescent point and to compare to calculated values.
- To measure the difference mode gain, the common mode gain, the common mode rejection ratio (CMRR) and to compare to calculated values.
- To understand the role of the common emitter resistor ( $R_E$ ) in providing feedback necessary for differential operation.
- To explore examples of applications of difference amplifiers.

### 2 Discussion

#### Notation:

In general, we use the upper case symbols, such as  $V$  and  $I$ , for the static or Q-point values of the voltages and currents. Similarly, we use the lower case symbols, such as  $v$  and  $i$ , for changes in the voltages and currents. Typical symbols for difference amplifiers, coupled for amplifying the difference between two AC signals, are shown.

Read Horowitz & Hill (2nd Ed) page 98. That description is for a DC coupled difference amplifier using +15 volt and -15 Volt power supplies. Our amplifier is for AC signals, and uses only one power supply but we use the same notation.

If a linear amplifier has two receiving input voltages  $v_i$  and  $v'_i$ , then its output may be a linear combination of the two inputs:

$$v_{out} = X.v_i + Y.v'_i$$

where  $X$  and  $Y$  are two constants. We can manipulate this equation to give

$$v_{out} = \frac{(X-Y)}{2}.(v_i - v'_i) + (X + Y).\frac{(v_i+v'_i)}{2}.$$

In other words,  $v_{out}$  can be written as the linear combination of the difference ( $v_i - v'_i$ ) and common mode or average  $\frac{(v_i+v'_i)}{2}$ .

The difference amplifier provides a number of advantages which make it one of the most useful circuit configurations, particularly as an input stage for high gain and DC amplifiers. By choosing matched transistors, often on the same piece of silicon of an integrated circuit, very stable and drift free operation may be obtained because of the symmetry of the amplifier. The differential input is particularly useful in cases where the desired signal is the difference between the voltages on two wires, which might be masked by a large and varying voltage, with respect to ground, that is common to both wires. Operational amplifiers often consist of a cascaded series of difference amplifiers which provide excellent stability and high gain. An ideal difference amplifier has a large gain for difference mode signals ( $v_i = -v'_i$ ), and

zero gain for common mode signals ( $v_i = v'_i$ ). We may write the output voltage (taken from either collector) for a real difference amplifier as:

$$v_{out} = A_d v_d + A_c v_c$$

where  $A_d$  is the difference mode gain and  $v_d = (v_i - v'_i)$  is the difference mode signal; and where  $A_c$  is the common mode gain and  $v_c = (v_i + v'_i)/2$  is the common mode signal.  $v_{out}$  is the voltage from output to ground, not the difference of  $v_{out}$  and  $v'_{out}$ .

If one uses only a difference mode signal (ie  $v_c = 0$ ), then  $A_d = v_o/v_d$ . For the common mode signal only ( $v_d = 0$ ), the common mode gain can be measured  $A_c = v_o/v_c$ .

A figure of merit for real difference amplifiers is called the *Common Mode Rejection Ratio*, CMRR, which is defined as:

$$CMRR = |A_d/A_c|$$

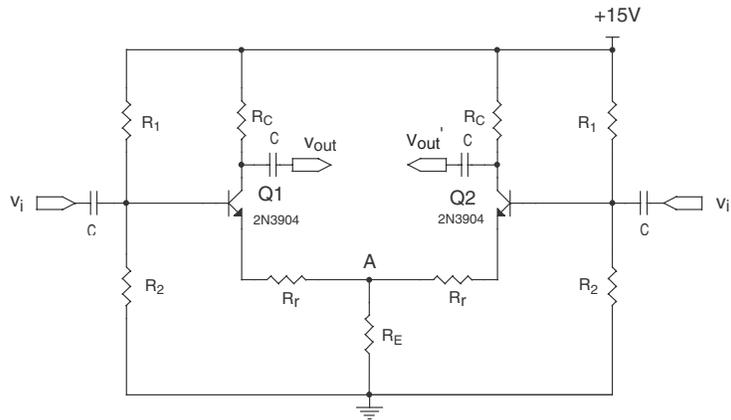


Figure 1: Schematic of the Difference Amplifier

For an ideal difference amplifier, CMRR would be infinite since  $A_c = 0$ , and for real amplifiers we want CMRR as large as possible. Consider the circuit shown in Figure 1. In the calculation sheet the gains and CMRR are derived and the results are:

$$A_d = -\frac{R_C}{2(R_r + r_{tr})}$$

$$A_c = -\frac{R_C}{2R_E + R_r + r_{tr}}$$

and

$$CMRR = \frac{2R_E + R_r + r_{tr}}{2(R_r + r_{tr})}$$

where  $r_{tr} = \text{transresistance} \simeq 0.025 \text{ ohm-amp}/I_c + 2 \text{ ohm}$ . (Sometimes this is given with mixed units:  $r_{tr} \simeq 25/I_c(mA) + 2 \text{ ohm}$ .) The symbol  $r_{tr}$  is sometimes written as  $r_e$ . The schematic in Fig. 1 does not explicitly show  $r_{tr}$ , but its value can simply be added to  $R_r$ .

It is apparent that CMRR will become larger as  $R_E$  becomes larger. The large  $R_E$  acts as a current source and an active current source, using an additional transistor is often used when a very large CMRR is desired. The effect of  $R_E$  may be understood by noting that, in the difference mode the currents in the two transistors are  $180^\circ$  out of phase, resulting in zero net AC current through  $R_E$ , thus making point A an AC ground (a virtual ground). This means a large difference mode gain. In the common mode, however, twice the AC current flows through  $R_E$  than through one transistor. In this case it appears that there is a resistor of value  $2R_E$  to ground and the common mode gain dramatically decreases. (For a true current source, the effective value of  $R_E \rightarrow \infty$ , giving  $A_c \sim 0$ .)

### 3 Procedure

This writeup contains a worksheet which will enable you to calculate the component values for the circuit. This must be done before the lab session.

1. Construct the circuit of Fig. 1. *Check the lead assignments for the 2N3904 on the data sheets which you will find in the lab.*
  - (a) Compare the measured values of  $V_b$ ,  $V_c$  and  $V_e$  to those calculated in the handout.
  - (b) Is your circuit balanced (ie  $V_c \approx V'_c$ )?
  - (c) Are both transistors turned on?
  - (d) *Use trimming resistors in parallel with the calculated bias resistors as necessary in order to balance – The collector currents should be the same within  $\approx 30\%$ .*
2. Generate a source of common and difference mode signals. One way to do this is to use the supplied transformer. When the center tap is grounded, the signal at the end of the winding is balanced such that the voltage on one side is equal to, but  $180^\circ$  out of phase with, that on the other. The difference input thus uses  $v_i$  from one side and  $v'_i$  from the other. The common-mode input uses both from the same side.
3.
  - (a) Using these signals, measure  $A_d$ ,  $A_c$  and the CMRR.
  - (b) Compare them to the calculated values.
  - (c) Note the relative phases of the signals at collectors of Q1 and Q2 and at point A.
4. The difference amplifier can be used with a one-sided input as a phase inverter.
  - (a) Feed an AC signal into the left input ( $v_i = \text{AC signal}$ ) and ground the right input ( $v'_i = 0$ ) through the coupling capacitor.
  - (b) Examine the outputs  $v_{out}$  and  $v'_{out}$  and the signal at point A.
  - (c) Explain why outputs  $v_{out}$  and  $v'_{out}$  have opposite polarity.
5. If there is time, you might measure the bandwidth of the amplifier.
  - (a) Use a one-sided input  $v_i$  as in 4a above *without* the transformer. Put a 3.3 k resistor in series with the input.

- (b) Measure the bandwidth.
- (c) Now put a 250 pF capacitor across the collector to the base of Q1.
- (d) Remeasure the bandwidth.
- (e) Then put a 1  $\mu$ F capacitor across  $R_C$  of Q1, examine the output at the collector of Q2 and again remeasure the bandwidth.
- (f) Discuss your observations.

## 4 Worksheet for the Difference Amplifier Laboratory

### 4.1 Calculation of the AC or Small Signal Gains

Refer to the difference amplifier circuit of Fig. 1. An AC equivalent circuit can be used to calculate the gains. To simplify the algebra we define  $R_f = r_{tr} + R_r$ . The gains and CMRR, which were derived before, can be rewritten:

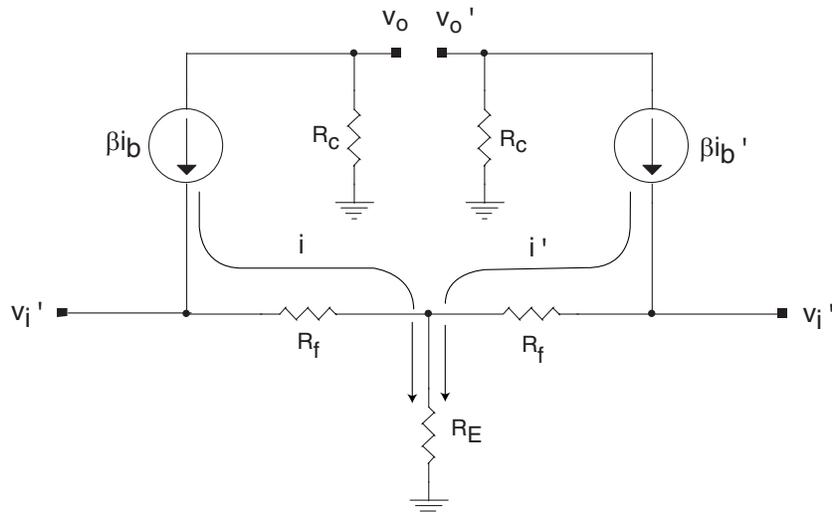
$$A_d = -\frac{R_C}{2R_f}$$

$$A_c = -\frac{R_C}{2R_E + R_f}$$

and

$$CMRR = \frac{2R_E + R_f}{2R_f}$$

Two current generators deliver currents  $i = \beta i_b$  and  $i' = \beta i'_b$  and we assume that  $\beta$  is large so that the base currents  $i_b$  and  $i'_b$  can be neglected and the emitter currents can be regarded as equal to the collector currents  $i_c$  and  $i'_c$ . Note that the inputs (the base connections) determine the voltages at the outer ends of the  $R_f$  resistors but do not supply an appreciable fraction of the current through them. (The base currents are only  $\frac{1}{\beta}$  of the collector currents.)



We can get 4 equations by applying ohm's law to this equivalent circuit.

$$v_i = (i + i')R_E + iR_f \quad (1)$$

$$v_i' = (i + i')R_E + i'R_f \quad (2)$$

$$v_o = -i R_C \quad (3)$$

$$v_o' = -i' R_C \quad (4)$$

A little algebra can be done on the 4 equations above to get them into the form  $v_o = A_d(v_i - v'_i) + A_c(v_i + v'_i)/2$ . Start with equation 1 minus equation 2 :

$$v_i - v'_i = (i - i') R_f \quad (5)$$

or

$$(i - i') = \frac{v_i - v'_i}{R_f} \quad (6)$$

Equation 3 minus equation 4 :

$$v_o - v'_o = -(i - i')R_C \quad (7)$$

Substituting equation 6 :

$$v_o - v'_o = -\frac{R_C}{R_f} (v_i - v'_i) \quad (8)$$

Equation 1 plus equation 2 gives:

$$v_i + v'_i = (i + i') (2R_E + R_f) \quad (9)$$

$$(i + i') = \frac{v_i + v'_i}{2R_E + R_f} \quad (10)$$

Equation 3 plus equation 4 gives:

$$v_o + v'_o = -(i + i') R_C \quad (11)$$

Substituting equation 10 :

$$v_o + v'_o = -\frac{R_C}{2R_E + R_f} (v_i + v'_i) \quad (12)$$

Adding equations 8 and 12 :

$$2v_o = -\frac{R_C}{R_f} (v_i - v'_i) - \frac{R_C}{2R_E + R_f} (v_i + v'_i) \quad (13)$$

or

$$v_o = \left[-\frac{R_C}{2R_f}\right] (v_i - v'_i) + \left[-\frac{R_C}{2R_E + R_f}\right] \frac{(v_i + v'_i)}{2} \quad (14)$$

We can define  $v_d = (v_i - v'_i)$  as the “Difference Mode” input voltage and define  $v_c = \frac{(v_i + v'_i)}{2}$  as the “Common Mode” input voltage.

Then equation 14 becomes

$$v_o = \left[-\frac{R_C}{2R_f}\right] (v_d) + \left[-\frac{R_C}{2R_E + R_f}\right] v_c \quad (15)$$

or

$$v_o = A_d \cdot v_d + A_c \cdot v_c \quad (16)$$

where

$A_d = -\frac{R_C}{2R_f}$  is the “Difference mode gain” and  $A_c = -\frac{R_C}{2R_E + R_f}$  is the “Common mode gain”.

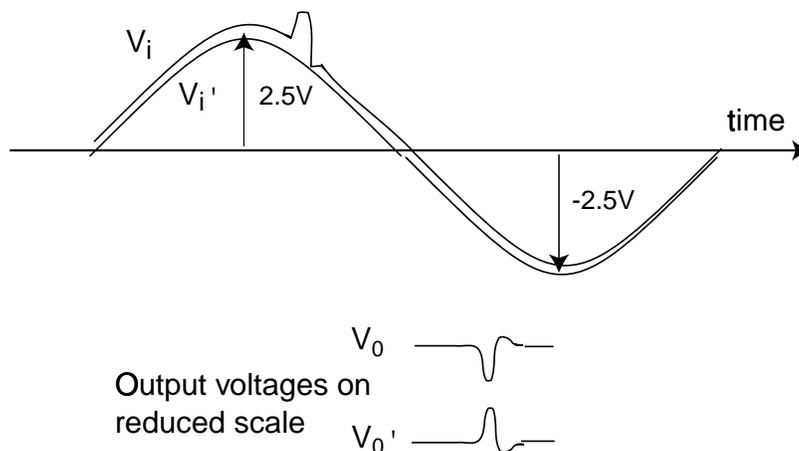
## 5 Calculation of the Component values

We want to meet the 5 following goals for the desired operating characteristics of the amplifier. Here we have picked a set of parameters for the design.

1. We want to use a single supply voltage with a voltage of  $V_{cc} = +15\text{ V}$ .
2. We want the Output impedance to be  $Z_{out} = 1\text{k}$ .
3. We want the Output Swing to be  $\pm 2\text{ V}$ .

(We define the “Output Swing” as the maximum voltage excursion which can be generated on each of the outputs without the amplifier becoming non-linear. The Output Swing of  $\pm 2\text{ V}$  means we would like the output  $v_o$  to be able to change by  $\pm 2\text{ V}$  and the output  $v'_o$  to be able to change by  $\pm 2\text{ V}$  with the outputs changing in opposite directions. Each output can change from its Q Point value by  $+2\text{ V}$  to  $-2\text{ V}$ , a difference of  $4\text{ V}$ . We say that the maximum “peak to peak output voltage” is  $v_{p-p} = \Delta v_c = 4\text{ V}$ . Thus each transistor must be able to operate in linear mode while its collector changes over a total range of  $4\text{ V}$ . We will also say that we want to do this while accommodating a common-mode input of up to  $\pm 2.5\text{ V}$ .)

4. The difference mode gain to be  $A_d \simeq 8$ .
5. We want the common mode gain  $A_c$  to be as low as possible, consistent with a common mode input range of  $\pm 2.5\text{ V}$ . That is, the  $\pm 2\text{ V}$  output swing should be available when the inputs are both  $2.5\text{ V}$  higher or lower than the “Q-point”. For example, if the two inputs are as shown, a difference amplifier will amplify the difference with a large gain and the average with small gain  $A_c$ .



You will meet these requirements with a circuit design where component values and operating point have been chosen as a suitable compromise between

- high difference mode gain
- low common mode gain
- desired range of output voltage swing and input common mode voltage
- and in some cases you might also need to consider other features such as power used, cost and physical size

The design choices to meet these goals are calculated below. You should follow this outline, make any necessary or suggested calculations and fill in the values in the next section.

1. First assume  $\beta$  is large to separate the tasks of
  - (a) first calculating the desired static voltages on the collectors, bases and emitters
  - (b) then, later in item 9, calculating the bias resistors  $R_1$  and  $R_2$  for each base
2. The output impedance assuming our Transistor Model (which assumes a current generator i.e. the impedance looking into the collector is high) is  $Z_{out} = R_C$ . To meet one of the goals, we choose  $R_C = 1$  k.
3. Since  $R_C = 1$  k and we want a 2 V output swing, we adopt the static current (ie average or DC current or quiescent) through each collector to be  $I_C = 2$  mA. The collector current of each transistor can then swing 2 mA between 0 mA and 4 mA.
4. Since an increase from 2 mA in one transistor will occur only when a decrease from 2 mA occurs in the other transistor, the common resistor  $R_E$  will carry a fairly constant 4 mA.
5. We can choose  $R_f$  to get the desired Difference Mode voltage Gain  $A_d = 8$ .
  - (a)  $A_d = R_C/2R_f$  and so  $R_f = \frac{R_C}{2A_d}$ .  
 Since we want  $A_d \simeq 8$ ,  
 we have  $R_f \simeq \frac{1.0 \text{ k}}{2 \times 8} = 62.5$  ohm.
  - (b) Since the base-emitter junction carries an average current of 2 mA,  
 $r_{tr} = (0.025 \text{ ohm-amp}/I_c) + 2$  ohm, and we have  
 $r_{tr} = \left(\frac{0.025}{0.002} + 2\right)$  ohm = 14.5 ohm.
  - (c) Since  $R_f = r_{tr} + R_r$ ,  $R_r$  should be about  $(62.5 - 14.5)$  ohm  $\approx 47$  ohm.
6. Use the following items to calculate  $R_E$ .
  - (a) We want the common mode gain  $A_c$  to be as low as possible consistent with other requirements:

$$A_c = -\frac{R_C}{2R_E + R_f}.$$

Therefore we would like to make  $R_E$  as large as practical. However, we must be careful to ensure the transistor remains in a linear mode and, for this, has  $V_C > V_E + 0.5$  volt at the extremes of our output swing.

- (b) The output swing of +2 V requires  $V_C \leq 13$  V at the Q point. From the symmetry of the circuit, we can see that  $V_E$  remains constant for a pure differential mode input. Therefore to get a downward 2 V swing,  $V_C$  needs to go to 11 V and  $V_E$  should be no higher than 10.5 V to avoid saturation.
- (c) However, we also need to allow for a  $\pm 2.5$  V common mode input at the same time.  $V_E$  follows  $v_i$ , so when the input common mode voltage goes to +2.5 V,  $V_E$  will be 2.5 V above the Q point. We can think of the common-mode input as a temporary shift in the Q point, and we still want to be able to see the output generated by our differential input signal without saturation or cutoff. So we need to pick a Q point that can be shifted  $\pm 2.5$  V and still allow our  $\pm 2V$   $V_C$  swing. So we should reduce our 10.5 V limit on the  $V_E$  Q point to 8 V to avoid saturation. (The negative excursion of the common mode input will make  $V_C$  rise a little due to the non-zero common mode gain. This will slightly reduce the available positive swing, but we will ignore this.)
- (d) The drop across  $R_r$  is only  $2 \text{ mA} \times 47 \text{ ohms} \approx 0.1$  V, so we want  $V_A \leq 8$  V at the Q point. Since the Q point current in  $R_E$  is 4 mA,  $R_E = \frac{8 \text{ volts}}{4 \text{ mA}} \approx 2$  k. However, our 10% resistors have standard values of 1.0, 1.2, 1.5, 1.8, 2.2, 2.7, 3.3, 3.9, 4.7, 5.6, 6.8, and 8.2 with any multiplier, so we choose the nearest standard value of resistor on the low side for  $R_E$  which is 1.8 k.

Now calculate your values for the Q point, starting with the standard resistor values you have chosen for the base bias, and using the the standard values for  $R_C$ ,  $R_r$ , and  $R_E$  determined above. These should be close to the desired voltages as derived in 2-6 above, but will differ because of the choice of standard resistor values.

$$\begin{aligned}
 V_B &= \text{-----} \text{ V.} \\
 V'_B &= \text{-----} \text{ V.} \\
 V_E &= \text{-----} \text{ V.} \\
 V'_E &= \text{-----} \text{ V.} \\
 V_A &= \text{-----} \text{ V.} \\
 V_C &= \text{-----} \text{ V.} \\
 V'_C &= \text{-----} \text{ V.}
 \end{aligned}$$

The bias network must now supply the appropriate  $V_B$ . We have a voltage for  $V_B$  of:  
 $V_E = 4 \text{ mA} \times 1.8 \text{ K} + \text{about } 0.1 \text{ V across } R_r + 0.7 V_{CE} \approx 8 \text{ V}$ . This gives the required ratio for  $R_1$  and  $R_2$  assuming that  $\beta \rightarrow \infty$ .

To allow for  $\beta_{min} = 75$ , we must limit the Thevenin impedance of the voltage divider. If we want the maximum change in the emitter Q point to be 0.2 V, then  $I_B = 2 \text{ mA}/75$  through the Thevenin impedance must produce a voltage drop of less than 0.2 V.

Use these values to calculate  $R_1$  and  $R_2$  and then choose the closest available values from the list of standard resistor values.

$$R_1 = \text{----- ohm}$$

$$R_2 = \text{----- ohm}$$

Calculate the expected  $A_c$  and  $A_d$  using the actual resistor values.

$$A_c = \text{-----}$$

$$A_d = \text{-----}$$