

## For Quartus II 13.1

# 1 Introduction

This tutorial explains how to use the SignalTap II feature within Altera's Quartus <sup>®</sup> II software. The SignalTap II Embedded Logic Analyzer is a system-level debugging tool that captures and displays signals in circuits designed for implementation in Altera's FPGAs.

SignalTap II

with Verilog Designs

### **Contents**:

- Example Circuit
- Using the SignalTap II Logic Analyzer
- Probing the Design Using SignalTap
- Advanced Trigger Options
- Sample Depth and Buffer Acquisition Modes

# 2 Background

Quartus<sup>®</sup> II software includes a system level debugging tool called SignalTap II that can be used to capture and display signals in real time in any FPGA design.

During this tutorial, the reader will learn about:

- Probing signals using the SignalTap software
- Setting up triggers to specify when data is to be captured

This tutorial is aimed at the reader who wishes to probe signals in circuits defined using the Verilog hardware description language. An equivalent tutorial is available for the reader who prefers the VHDL language.

The reader is expected to have access to a computer that has Quartus II software installed. The detailed examples in the tutorial were obtained using Quartus II version 13.1, but other versions of the software can also be used.

### Note:

Please note that there are no red LEDs on a DE0 or DE0-Nano board. All procedures using red LEDs in this tutorial are to be completed on the DE0 or DE0-Nano boards using green LEDs instead. If you are doing this tutorial on a DE0 board, replace *LEDR* with *LEDG* in the Verilog modules below. If you are foing this tutorial on a DE0-Nano board, replace *LEDR* with *LED* below.

Additionally, the DE0-Nano is limited to 4 switches. If you are doing this tutorial on a DE0-Nano, replace all occurances of [7:0] with [3:0] below.

# 3 Example Circuit

As an example, we will use the switch circuit implemented in Verilog in Figure 1. This circuit simply connects the first 8 switches on the DE-series board to the first 8 red LEDs on the board. It does so at the positive edge of the clock (CLOCK\_50) by loading the values of the switches into a register whose output is connected directly to the red LEDs.

// Top-level module
module switches (SW, CLOCK\_50, LEDR);
input [7:0] SW;
input CLOCK\_50;
output reg [7:0] LEDR;

**always** @(posedge CLOCK\_50) LEDR [7:0] <= SW [7:0]; **endmodule** 

Figure 1. The switch circuit implemented in Verilog code

Implement this circuit as follows:

- Create a project *switches*.
- Include a file *switches.v*, which corresponds to Figure 1, in the project.
- Select the correct device that is associated with the DE-series board. A list of device names for DE-series boards can be found in Table 1.
- Import the relevant qsf file. For example, for a DE2-115 board, this file is called *DE2-115.qsf* and can be imported by clicking Assignments > Import Assignments. For convenience, this file is provided in the *design\_files* subdirectory within the tutorials folder, which is included on the CD-ROM that accompanies the DE-series board and can also be found on Altera's DE-series web pages. The node names used in the sample circuit correspond to the names used in this file.
- Compile the design.

Board	Device Name
DE0	Cyclone III EP3C16F484C6
DE0-Nano	Cyclone IVE EP4CE22F17C6
DE1-SoC	Cyclone V SoC 5CSEMA5F31C6
DE2-115	Cyclone IVE EP4CE115F29C7

Table 1. DE-series FPGA device names

# 4 Enabling the Quartus II TalkBalk Feature

When using the Quartus II Web Edition, the TalkBack feature must be enabled in order to access the SignalTap II software. Enabling TalkBack allows Quartus II and other Altera programs to send a limited amount of data regarding

their usage to Altera. This data is primarily used to better understand how users interact with the software, and does not include any design files. The full list of what data is or is not sent can be found in the TalkBack License Agreement.

To enable the TalkBack feature in Quartus II, select Tools > Options. In the Options window, select Internet Connectivity from the menu, and click on TalkBack Options... to open the window shown in Figure 2. If you accept the TalkBack License Agreement, then check the box labelled Enable sending TalkBack data to Altera and click OK.

Quartus II TalkBack
Enable Advanced
QUARTUS II SOFTWARE - TALKBACK FEATURE
INTRODUCTION
The TalkBack feature, included with the Licensed Program(s), enables ALTERA to receive limited information concerning the Licensed Program(s) that you use and your compilation of logic designs (but not the logic design files themselves) using the Licensed Program(s). One of the primary purposes of the TalkBack feature is to assist ALTERA in understanding how its customers use the Licensed Program(s) and ALTERA's other products, so more effort can be placed on improving the features most important to users. To disable/enable the TalkBack feature, run tb2_install.exe (or just tb2_install in Linux) located in your quartus/bin folder.
Enable sending TalkBack data to Altera
OK Cancel Help

Figure 2. Enabling the TalkBack feature.

# 5 Using the SignalTap II software

In the first part of the tutorial, we are going to set up the SignalTap Logic Analyzer to probe the values of the 8 LED switches. We will also set up the circuit to trigger when the first switch (LED[0]) is high.

1. Open the SignalTap II window by selecting File > New, which gives the window shown in Figure 3. Choose SignalTap II Logic Analyzer File and click OK.

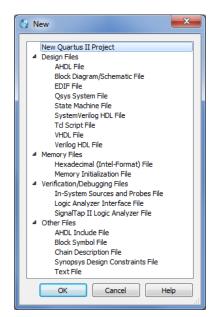


Figure 3. Need to prepare a new file.

2. The SignalTap II window with the Setup tab selected is depicted in Figure 4. Save the file under the name *switches.stp*. In the dialog box that follows (Figure 5), click OK. For the dialog "Do you want to enable SignalTap II file 'switches.stp' for the current project?" click Yes (Figure 6). The file *switches.stp* is now the SignalTap file associated with the project.

Note: If you want to disable this file from the project, or to disable SignalTap from the project, go to Assignments > Settings. In the category list, select SignalTap II Logic Analyzer, bringing up the window in Figure 7. To turn off the analyzer, uncheck Enable SignalTap II Logic Analyzer. Also, it is possible to have multiple SignalTap files for a given project, but only one of them can be enabled at a time. Having multiple SignalTap files might be useful if the project is very large and different sections of the project need to be probed. To create a new SignalTap file for a project, simply follow Steps 1 and 2 again and give the new file a different name. To change the SignalTap file associated with the project, in the SignalTap II File name box browse for the file wanted, click Open, and then click OK. For this tutorial we want to leave SignalTap enabled and we want the SignalTap II File name to be *switches.stp*. Make sure this is the case and click OK to leave the settings window.

w	Sig	nalTap I	Logic Analyzer - I	D:/signalt	tapintro_veri	log/switches - sw	vitches - [switches	.stp]				
Fil	e	Edit V	ew Project Pro	cessing	Tools Wind	dow Help 🐬				Se	arch altera.	com 🔇
In	istan	ce Mana	ger: 📉 🔊 🔳	📘	Add nodes to	the current instand	ce .	0	×	JTAG Chain Configuration: JTAG rea	dy	×
Ins	stand		Status g Not running	LEs: 0 ce		Memory: 0 0 bits	Small: NA	Med NA	um: NA	Hardware: USB-Blaster [USB-0]	•	Setup
		auto_s	g Not running	0 ce	llS	0 bits	NA	NA		Device: @1: EP2C35 (0x020B40D	D) 🔻	Scan Chain
•					III				4	>> SOF Manager:		
1	_				(	<b>•••</b>			<i>c</i> . 1	0.0		
ľ	aut	o_signal	Node		Lock mode: Data Enable	Allow all chang	rigger Condition	• •	Signal	Configuration:		×
	Тур	e Alias			0	0	1 V Basic	•	Clock:			E
		Data	ead nodes						Sam	nple depth:     128     RAM type:     #       Segmented:     2     64 sample segments       torage qualifier:	uto	<b>v</b>
ŀ	Hiera	rchy Dis			×							×
						👯 auto_signalta	p_0					
	<b>&amp;</b> a	auto_sign	altap_0								0%	00:00:00

Figure 4. The SignalTap II window.



Figure 5. Click OK to this dialog.



Figure 6. Click Yes to this dialog.

P Settings - switches		- • ×
Category:		Device
General	SignalTap II Logic Analyzer	
Files Libraries Operating Settings and Conditions	Specify compilation options for the SignalTap II Logic Analyzer.	
Voltage Temperature	V Enable SignalTap II Logic Analyzer	
<ul> <li>Compilation Process Settings Early Timing Estimate Incremental Compilation Physical Synthesis Optimizations</li> <li>EDA Tool Settings Design Entry/Synthesis Simulation Formal Verification Board-Level</li> <li>Analysis &amp; Synthesis Settings VHDL Input Verilog HDL Input Default Parameters</li> <li>Fitter Settings TimeQuest Timing Analyzer Assembler Design Assistant</li> <li>SignalTap II Logic Analyzer Logic Analyzer Interface PowerPlay Power Analyzer Settings SSN Analyzer</li> </ul>	SignalTap II File name: switches.stp	
	OK Cancel Apply	Help

Figure 7. The SignalTap II Settings window.

3. We now need to add the nodes in the project that we wish to probe. In the Setup tab of the SignalTap II window, double-click in the area labeled Double-click to add nodes, bringing up the Node Finder window, as shown in Figure 8. Click on ≥ to show more search options. For the Filter field, select SignalTap II: pre-synthesis, and for the Look in field select |switches|. Click List. This will now display all the nodes that can be probed in the project. Highlight SW[0] to SW[7], and then click the > button to add the switches to be probed. Then click OK.

Named:	*					•		List 🔿
Options								
Filter:	SignalTap II: pre-syr	nthesis					•	Customize
Look in:	switches				🗸	Include subentities	<b>V</b>	Hierarchy view
Nodes Fo	und:	+:	-:		Selected Nod	es:		
	Name	Assignments	*	\$		Name		Assignments
	LEDR[7]	PIN_AC21			in		PIN	N25
	LEDR[7]~reg0	Unassigned			in SW[1]		PIN_	_N26
	SW	Unassigned			in_ SW[2]		PIN	P25
	SW[0] SW[1]	PIN_N25 PIN_N26			- SW[3]			
	SW[1] SW[2]	PIN_126		>>	in_ sw[4]			AF14
	SW[3]	PIN AE14	_	$\overline{\langle}$	- SW[5]			AD13
	SW[4]	PIN_AF14		<	in SW[6]			AC13
	SW[5]	PIN_AD13	Ε		- SW[0]			C13
	SW[6]	PIN_AC13			- 3W[/]		FUN_	
<b>B</b> -	SW[7]	PIN_C13	-					
4			Ψ.	<b> </b> ¢	•			•

Figure 8. Adding nodes in the Node Finder window on a DE-series board.

4. Before the SignalTap analyzer can work, we need to specify what clock is going to run the SignalTap module that will be instantiated within our design. To do this, in the Clock box of the Signal Configuration pane of the SignalTap window, click ..., which will again bring up the Node Finder window. Select List to display all the nodes that can be added as the clock, and then double-click CLOCK\_50, which results in the image shown in Figure 9. Click OK.

Named:	•					•	List 📝
Options							
Filter:	SignalTap II: pre-sy	nthesis					▼ Customize
Look in:	switches				▼ ▼	Include subentities	Hierarchy view
Nodes Fou	nd:		=:		Selected Node	s:	
	Name	Assignments		¢ 🛛		Name	Assignments
	LOCK_50 EDR EDR[0] EDR[1] EDR[1] EDR[2] EDR[2] EDR[3]	PIN_N2 Unassigned PIN_AE23 Unassigned PIN_AF23 Unassigned PIN_AB21 Unassigned PIN_AC22 Unassigned PIN_AC22	F	> >> <<			PIN_N2

Figure 9. Setting CLOCK\_50 as the clock for the SignalTap instance on a DE-series board.

5. With the Setup tab of the SignalTap window selected, select the checkbox in the Trigger Conditions column. In the dropdown menu at the top of this column, select Basic AND. Right-click on the Trigger Conditions cell corresponding to the node SW[0] and select High. Now, the trigger for running the Logic Analyzer will be when the first switch on the DE-series board is set to high, as shown in Figure 10. Note that you can right click on the Trigger Conditions cell of any of the nodes being probed and select the trigger condition from a number of choices. The actual trigger condition will be true when the logical AND of all these conditions is satisfied. For now, just keep the trigger condition as SW[0] set to high and the others set to their default value, Don't Care.

auto_	signalt	ap_0	Lock mode:	鹶 Allow all chang	es
		Node	Data Enable	Trigger Enable	Trigger Conditions
Туре	Alias	Name	8	8	1 🔽 Basic AND 🛛 🔻
in		SW[0]	<b>V</b>	<b>V</b>	1
in		SW[1]	<b>V</b>	<b>V</b>	
in		SW[2]	<b>V</b>	<b>V</b>	
in_		SW[3]	<b>V</b>	<b>V</b>	
in_		SW[4]	<b>V</b>	<b>V</b>	
in_		SW[5]	<b>V</b>	<b>V</b>	
in		SW[6]	<b>V</b>	<b>V</b>	
in		SW[7]	<b>V</b>		22

Figure 10. Setting the trigger conditions.

6. For SignalTap II to work, we need to properly set up the hardware. First, make sure the DE-series board is plugged in and turned on. In the Hardware section of the SignalTap II window, located in the top right corner, click Setup..., bringing up the window in Figure 11. Double click USB-Blaster in the Available Hardware Items menu, then click Close.

Hardware Setup			-								
Hardware Settings JTAG S	ettings										
Select a programming hardware setup to use when programming devices. This programming hardware setup applies only to the current programmer window.											
Currently selected hardware:	USB-Blaster [USB-0]		-								
Available hardware items											
Hardware	Server	Port	Add Hardware								
USB-Blaster	Local	USB-0	Remove Hardware								
			Close								

Figure 11. Setting up hardware.

7. The last step in instantiating SignalTap in your design is to compile the design. In the main Quartus II window, select Processing > Start Compilation and indicate that you want to save the changes to the file by clicking Yes. After compilation, go to Tools > Programmer and load the project onto the DE-series board.

# 6 Probing the Design Using SignalTap II

Now that the project with SignalTap II instantiated has been loaded onto the DE-series board, we can probe the nodes as we would with an external logic analyzer.

- 1. On the DE-series board, first set all of the switches (0-7) to low. We will try to probe the values of these switches once switch 0 becomes high.
- 2. In the SignalTap window, select Processing > Run Analysis or click the 🗟 icon. Then, click on the Data tab of the SignalTap II Window. You should get a screen similar to Figure 12. Note that the status column of the SignalTap II Instance Manager pane says "Waiting for trigger." This is because the trigger condition (Switch 0 being high) has not yet been met. (This is of course if Switch 0 is actually low as instructed in the previous step. If it is not, set it to low and then click Run Analysis again).

nstanc	e Manag	er: 🍡 🔊 🔳	Acc	uisition in progress			JTAG Chain	Configuration: ]	/TAG ready		
stance		Status g Waiting for trigge	LEs: 49 er 495 cell		4 Small: 0/0 0 blocks	Me 1t	Device:	USB-Blaster [USB @1: EP2C35 (0xi Manager:	020B40DD)		Setup Scan Chain
						r					
log:	2012/11	/01 14:25:34 #0				click to ins	ert time bar				
Type	Alias	Name	0	8 16 24	32 40 48	56	64 72	80 88 9	96 104	112	120 128
in		SW[0]	A	cquisition in progress	.1				hantinter		
in		SW[1]									
in		SW[2]									i
in		SW[3]									i
in		SW[4]									
in		SW[5]									
in		SW[6]									i
in		SW[7]									
·	Data chy Disp			X Data Log:	9						×
💦 aı	uto_sign:	altap_0									
									1	00%	00:00:4

Figure 12. SignalTap II window on a DE-series board after Run Analysis has been clicked.

3. Now, to observe the trigger feature of the Logic Analyzer, set Switch 0 on the DE-series board to high. The data window of the SignalTap II window should display the image in Figure 13. Note that this window shows the data levels of the 8 nodes being tapped before the trigger condition was met and also after. To see this, flip on any of the switches from 0-7 and then click Run Analysis again. When switch 0 is set to high again, you will see the values of the switches displayed on the SignalTap II Logic Analyzer.

	w Project Proces	sing loois wi	ndow Help 🐬			Search altera.com
nstance Manage	er: 🍡 🔊 🔳	Ready to ac	quire		X	JTAG Chain Configuration: JTAG ready
stance	Status	LEs: 495	Memory: 1024	Small: 0/0	Me	e Hardware: USB-Blaster [USB-0] ▼ Setup
🚼 auto_sig	Not running	495 cells	1024 bits	0 blocks	11	
						Device: @1: EP2C35 (0x020B40DD)  Scan Chain
						>> SOF Manager: 🔔 🕕 butput_files/switches.sof
		III			P.	
					dan ta	and the last
	01 14:25:34 #0	40 0	0 0 40			nsert time bar 48 56 64 72 80 88 96 104 112
Type Alias	Name	-16 -8	0 8 16		40 4	48 56 64 72 80 88 96 104 112
	SW[0]		_			
	SW[1]					
	SW[2]		_			
	SW[3]					
	SW[4]					
	SW[5]		_			
	SW[6]					
in	SW[7]					
🔊 Data	setup					
Hierarchy Displa		×	🛛 Data Log: 📑			~
	-			-		×
🔽 🎐 swi	tcnes		🗞 auto_signaltap	_0		

Figure 13. Graphical display of values after trigger condition is met.

# 7 Advanced Trigger Options

Sometimes in a design you may want to have a more complicated triggering condition than SignalTap's basic triggering controls allow. The following section describes how to have multiple trigger levels.

### 7.1 Multiple Trigger Levels

In this section, we will set up the analyzer to trigger when there is a positive edge from switch 0, switch 1, switch 2, and then switch 3, in that order.

- 1. Click the Setup tab of the SignalTap II window.
- 2. In the Signal Configuration pane, select 4 from Trigger Conditions dropdown menu as in Figure 14 (you may have to scroll down in the Signal Configuration pane to see this menu). This modifies the node list window by creating three new Trigger Conditions columns.

Trigger	
Trigger flow control:	Sequential 🔹
Trigger position:	₽re trigger position
Trigger conditions:	4
Trigger in	
O Pin:	
O Node:	
Instance:	•
Hard Processor	r System (HPS) trigger out
Pattern:	High 👻
Trigger out	
Pin:	
Instance:	<b>•</b>
Hard Processor	System (HPS) trigger in
Hard Processor	System (HPS) event: 0 💌
Level:	Active High
Latency delay: 5	cydes

Figure 14. Set trigger levels to 4.

3. Right click the Trigger Condition 1 cell for SW[0], and select Rising Edge. Do the same for the Trigger Condition 2 cell for SW[1], Trigger Condition 3 for SW[2], and Trigger Condition 4 for SW[3]. You should end up with a window that looks like Figure 15.

trigge	er: 2012	2/11/01 14:22:59 #1	Lock mode:	鹶 Allow all chang	es	•					
		Node	Data Enable	Trigger Enable	rigger Enable Trigger Conditions						
Туре	Alias	Name	8	8	1 🔽 Basic 🔹 🔻	2 🔽 Basic 🔹	3 🔽 Basic 🔹 🔻	4 🔽 Basic 🔹			
in		SW[0]	<b>V</b>	<b>V</b>	5						
in		SW[1]	<b>V</b>	<b>V</b>		5					
in		SW[2]	<b>V</b>	<b>V</b>			5				
in		SW[3]	<b>V</b>	<b>V</b>				5			
in		SW[4]	<b>V</b>	<b>V</b>							
in		SW[5]	<b>V</b>	<b>V</b>							
in		SW[6]	<b>V</b>	<b>V</b>							
in		SW[7]	<b>V</b>	<b>V</b>							

Figure 15. Multiple trigger levels set.

- 4. Now, recompile the design and load it onto the DE-series board again.
- 5. Go back to the SignalTap II window, click on the Data tab, and then click Processing > Run Analysis. Note that the window will say "Waiting for trigger" until the appropriate trigger condition is met. Then, in sequence, flip to high switches 0, 1, 2, and then 3.

After this has been done, you will see the values of all the switches displayed as in Figure 16. Experiment by following the procedure outlined in this section to set up other trigger conditions and use the DE-series board to test these trigger conditions.

If you want to continuously probe the analyzer, instead of clicking "Run Analysis," click "Autorun Analysis" which is the icon right next to the "Run Analysis" icon. If you do this, every time the trigger condition is met the value in the display will be updated. You do not have to re-select "Run Analysis." To stop the "Autorun Analysis" function, click the **I** icon.

log: 2	log: 2012/11/02 17:16:57 #0				dick to insert time bar															
Туре	Alias	Name	-16	-8		0 1	. 8	16	24	32	40	48	56	64	72	80	88	96	104	112
in		SW[0]																		
in		SW[1]				1														
in		SW[2]																		
in		SW[3]																		
in		SW[4]																		
in		SW[5]																		
in		SW[6]																		
in		SW[7]																		

Figure 16. Logic Analyzer display when all four trigger conditions have been met.

## 7.2 Advanced Trigger Conditions

In this section we will learn how to create advanced trigger conditions. Our trigger condition will be whenever any one of the first 3 LED displays have a positive or negative edge. This means that the Logic Analyzer will update its display every time one of these inputs changes. Note that we could have any logical function of the nodes being probed to trigger the analyzer. This is just an example. After you implement this in the next few steps, experiment with your own advanced triggers.

- 1. Have the *switches* project opened and compiled from the previous examples in this tutorial.
- 2. Open the SignalTap window and select the Setup tab. In the Signal Configuration pane make sure that the number of Trigger Conditions is set to 1.
- 3. In the Trigger Conditions column of the node list, make sure the box is checked and select Advanced from the dropdown menu as in Figure 17. This will immediately bring up the window in Figure 18. This window allows you to create a logic circuit using the various nodes that you are probing with SignalTap.

trigge	er: 2012	2/11/01 14:37:50 #0	Lock mode:	k mode: 📄 Allow all changes						
		Node	Data Enable	Trigger Enable	Trigger Conditions					
Туре	Alias	Name	8	8	1 🔽 Basic 🔹 🔻					
in		SW[0]	<b>V</b>	<b>V</b>	Basic Advanced					
in		SW[1]	<b>V</b>	<b>V</b>						
in		SW[2]	<b>V</b>	<b>V</b>						
in		SW[3]	<b>V</b>	<b>V</b>						
in		SW[4]	<b>V</b>	<b>V</b>						
in		SW[5]	<b>V</b>	<b>V</b>						
in		SW[6]	<b>V</b>	<b>V</b>						
in		SW[7]	<b>V</b>	<b>V</b>						

Figure 17. Select Advanced from the Trigger Level dropdown menu.

Node	List:			Advanced Trigger Condition Editor: Condition 1	
Туре	Alias	Name		Result:	*
in		SW[0]	•		
in 👝		SW[1]			
in		SW[2]	-		
<u> </u>	t Librar			–∋ Result	E
	_	& Level Detector	<u>^</u>		
		t Objects			
		parison Operators	E		
⊳∍	<ul> <li>Bitwis</li> </ul>	se Operators			
⊳ ⇒	- Logic	al Operators		Object has an incorrect number of inputs.	-
⊳∍	- Redu	iction Operators	-	•	•
🔊 D	ata	🔜 Setup 🐻 Ad	vanced Trigger 1		

Figure 18. The Advanced Trigger editing window.

4. In the node list section of this window, highlight the 3 nodes SW[0] to SW[2], and click and drag them into the white space of the Advanced trigger window, resulting in Figure 19. Note that you can also drag and drop each node individually.

Node	List:			Advanced Trigger Condition	Editor: Condition 1			
Туре	Alias	Name		Result:				*
in		SW[0]		SW[1]	SW[0] G-			
in_		SW[1]		SW[2]		= Result		
in		SW[2]	-	SW[0]	SW[1] G-	Result		
Object Library:					SW[2] G			
=1	⊢ Edge	& Level Detector	*					Ξ
⊳⊫	⊢ Inpu	t Objects						
⊳∍	Comp	parison Operators	=					
⊳∍	⊢ Bitwi	se Operators						
⊳∍	⊢ Logio	cal Operators		Object has an incorrect numb	er of inputs.			Ŧ
⊳∍	⊢ Redu	uction Operators	-	•		III	•	
- 🔊 D	ata	a Setup 🐻 Ad	vanced Trigger 1					

Figure 19. The three input nodes of interest dragged into the Advanced Trigger Editing Window.

5. We now need to add the necessary logical operators to our circuit. We will need an OR gate as well as three edge level detectors. To access the OR gate, click on the plus sign next to Logical Operators in the Object Library and select Logical Or, as in Figure 20. Then drag and drop the operator into the editing window.

Object Library:	
▲ ⇒ Logical Operators	*
Logical Not	
Logical And	
Logical Or	=
Logical Xor	
Reduction Operators	-

Figure 20. Select the Logical Or operator from the Object Library window and drag this into the editing window.

6. In the object library click Edge and Level Detector and drag this into the editing window. Do this three

times and then arrange the circuit as in Figure 21. The three inputs should each be connected to the input of an edge and level detector and the output of each of these detectors should be connected to the OR gate. The output of the OR gate should be connected to the output pin already in the editing window.

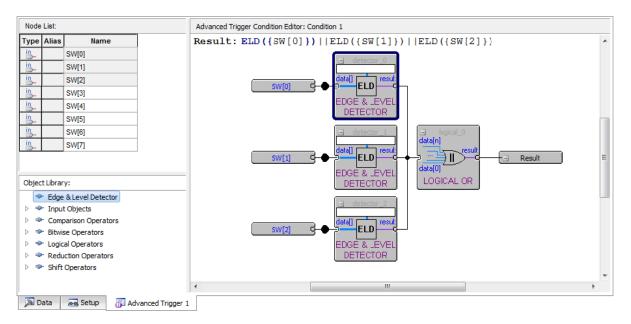


Figure 21. Arrange the elements to create a circuit that looks like this.

7. We now need to set each edge and level detector to sense either a falling edge or a rising edge. Double click one of the edge and level detectors, bringing up the window in Figure 22. Type E in the setting box and then click OK. This will mean that the detector will output 1 whenever there is either a falling edge or a rising edge of its input. Repeat this step for the two remaining edge and level detectors.

Parameter		Reset		
Name:	Edge & Level Dete	ector Pattern		Reset All
Setting:	E		-	Reset All
	Allow this sett	ing to be configurable at	runtime	
Description:	inputs. Create p legal characters:	tern used to compare wi atterns using the followir 1=High, 0=Low, H=Higl gEdge, F=Falling Edge,	ng 🗍	
Existing param	neter settings:			
Name		Setting	Configu	urable at Rur
Name				
	Detector Pattern	E	Always	
	Detector Pattern	E 0	Always Never	

Figure 22. Type E in the setting box so that the function triggers on both rising and falling edges.

8. To test this Advanced trigger condition, compile the designed circuit again and load it onto the DE-series board. Then run Signal Tap as described in the previous section. You should note that the Analyzer should sense every time you change one of the first three switches on the board.

## 8 Sample Depth and Buffer Acquisition Modes

In this section, we will learn how to set the Sample Depth of our analyzer and about the two buffer acquisition modes. To do this, we will use the previous project and use segmented buffering. Segmented buffering allows us to divide the acquisition buffer into a number of separate, evenly sized segments. We will create a sample depth of 256 bits and divide this into eight 32-sample segments. This will allow us to capture 8 distinct events that occur around the time of our trigger.

- 1. Change the trigger condition back to Basic and have only one trigger condition. Make the trigger condition to be at either edge of SW[0].
- 2. In the Signal Configuration pane of the SignalTap II window, in the Sample depth dropdown menu of the Data pane select 256. This option allows you to specify how many samples will be taken around the triggers in your design. If you require many samples to debug your design, select a larger sample depth. Note, however, that if the sample depth selected is too large, there might not be enough room on the board to hold your design and the design will not compile. If this happens, try reducing the sample depth.
- In the Signal Configuration pane of the SignalTap II window, in the Data section of the pane check Segmented. In the dropdown menu beside Segmented, select 8 32 sample segments. This will result in a pane that looks like Figure 23.

#### SIGNALTAP II WITH VERILOG DESIGNS

k: CLOCK_50									
ata									
ample depth: 2	56 🔹 RAM type:	Auto							
Segmented:	8 32 sample segments								
Storage qualifier	r:								
Type:	Continuous	-							
Input port: au	to_stp_external_storage_	qualifier							
✓ Record data	discontinuities								
Disable store	age qualifier								
igger									
igger flow contr	ol: Sequential								
igger position:	🗱 Pre trigger positio	Pre trigger position							
igger conditions	: [1								
Trigger in									
O Pin:									
Node:									
Instance:		~							
Hard Proces	sor System (HPS) trigger out								
Pattern:	1 High	-							
Trigger out									
Pin:									
Instance:		~							
Hard Proces	sor System (HPS) trigger ir	1							
Hard Proces	sor System <mark>(</mark> HPS) event:	0 -							
Level:	Active High	-							
Latency delay:	5 cycles								

Figure 23. Select Segmented buffer acquisition mode with 8 32 sample segments.

- 4. Recompile and load the designed circuit onto the DE-series board. Now, we will be able to probe the design using the Segmented Acquisition mode.
- 5. Go back to the SignalTap II window and click Processing > Run Analysis. Now, flip SW[0] up and down, and in between flips change the values of the other 7 switches. After you have done this 8 times, the values in the buffer will be displayed in the data window, and this will display the values that the 8 switches were at around each trigger. A possible waveform is presented in Figure 24. This resulted from the user flipping up one more switch between each flip of SW[0].

		Node	0		1	:	2	3	4		5		6		7		8
Туре	Alias	Name	-4	12	-4	12 -	4	12 -4	12 -4		12 -4	12	-4	12	-4	12	0
in		SW[0]	Ц														
in		SW[1]								1							
in		SW[2]	L														
in		SW[3]	L							1							
in		SW[4]	L														
in		SW[5]	E							1							
in 👝		SW[6]	L														
in		SW[7]					i i			i i	1	i					_

Figure 24. Possible waveforms that could result when using the Segmented Acquisition mode.

#### 8.1 Use of Synthesis Keep Directive

Sometimes a design you create will have wires in it that the Quartus compiler will optimize away. A very simple example is the Verilog code below:

module threeInputAnd(SW, LEDR, CLOCK\_50);
input CLOCK\_50;
input [2:0] SW;
output reg [0:0] LEDR;
wire ab, abc /\*synthesis keep\*/;
assign ab=SW[0]&SW[1];
assign abc=ab&SW[2];
always @ (posedge CLOCK\_50)
begin
 LEDR[0]<=abc;
end
endmodule</pre>

Figure 25. Using the Synthesis Keep directive in Quartus II.

A diagram of this circuit is shown in Figure 26. The triangular symbols labeled **ab** and **abc** are buffers inserted by Quartus. They do not modify the signals passing through them.

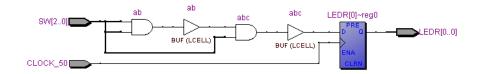


Figure 26. The circuit implemented by the code in Figure 25

We wish to instantiate a SignalTap II module that will probe the values of the inputs SW[2:0] and the outputs LEDR[2:0]. We also want to probe the internal wire **ab**. However, normally when this Verilog code is compiled (without the /\*synthesis keep\*/ directive), the wire **ab** is optimized away into one logic element, as in Figure 27.

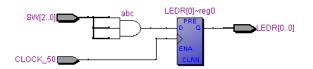


Figure 27. The same circuit without the Synthesis Keep directive.

If you wish to probe this internal wire, however, you will have to direct Quartus that you do not want this wire to be optimized away. To do so, place the text /\**synthesis keep*\*/ on the line that declares the wire, right before the semicolon of the line. Figure 25 already contains this directive. We will now demonstrate how this wire can be probed:

- 1. Create a new Quartus project threeInputAnd and copy the Verilog code from Figure 25. Compile the project.
- 2. Go to Tools > SignalTap II Logic Analyzer, and then in the Setup pane of the SingalTap II window, right click and choose Add Nodes.
- For the Filter field, select SignalTap II: pre-synthesis. Select |threeInputAnd| in the Look in drop-down menu and click the List button. Move the nodes ab, SW[0], SW[1], SW[2], and LEDR[0] into the Selected Nodes list and then click OK.
- 4. In the Signal Configuration pane, select CLOCK\_50 as the clock signal.
- 5. Set a Trigger Condition to trigger when **ab** becomes high.
- 6. Import the relevant pin assignment file for the DE-series board (or assign the pins manually, as described in Section 7 of the Quartus II Introduction tutorials). For a DE2-115 board, this file is named *DE2-115.qsf*
- 7. Compile the project again.
- 8. Go to Tools > Programmer and load the circuit onto the DE-series board.

- 9. Open the SignalTap window again, and select the Data tab. Set all the switches on the DE-series board to the low position. Then, start the analysis by selecting Processing > Run Analysis.
- 10. Set the first two switches to the high position. The Trigger Condition should be satisfied.

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