Use '193 LOAD' input to pin counter to load value during times when this state has not been selected by the TOP-level FSM. When the state is selected the LOAD' is pulled high for the period of that state. The counter counts until decrementing through 0 when BO' is asserted for $1 / 2$ (!!) clock cycle. This is actually unfortunately limiting the maximum CLK frequency of this circuit to about 2.5 MHz

CLK
WAIT500


## Title Binary Counters

| Size | $\begin{array}{l}\text { Document Number } \\ \text { A }\end{array}$ |
| :---: | :--- |
| <Doc> |  |


Implementation = DS_RST

Implementation = DS_S1

STARTVAL = 0
OPPVAL = 1


