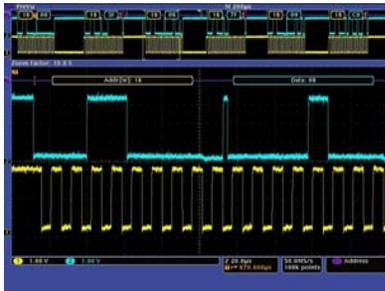


Overview of Common Serial Buses



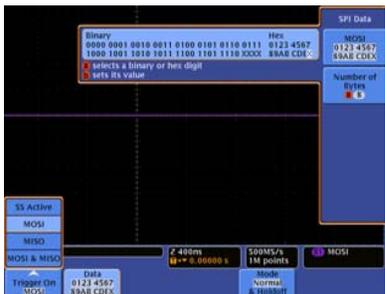
I²C (Inter-IC Bus)

- Used for chip-to-chip communication
- Uses two single-ended signals: clock and data



I²S / LJ / RJ / TDM Audio Buses

- I²S, Left Justified, and Right Justified used for stereo digital audio communication
- TDM supports >2-channel digital audio



SPI (Serial Peripheral Interface)

- Used to communicate between microcontrollers and their immediate peripheral devices
- Can use 2-, 3-, or 4-wire bus topology



CAN / LIN

- CAN used for system to system communication
- LIN used for low-cost, low-speed automotive communication



RS-232/422/485/UART

- Used for chip-to-chip and system-to-system communication
- Single-wire or differential signals
- Data is simultaneously transmitted and received

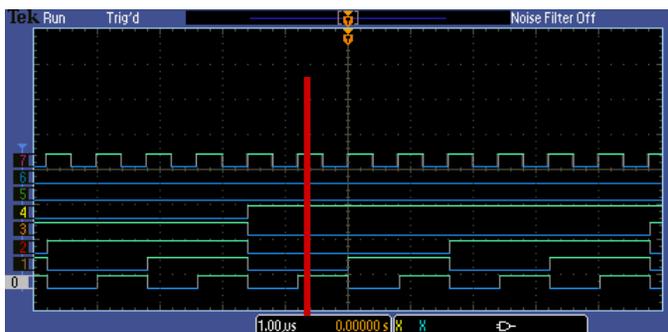


FlexRay

- Used for high-speed, high-reliability automotive communication
- Differential signaling, at rates up to 10 Mbps

Overview of Parallel Buses

With a parallel architecture, each component of the bus has its own signal path. There may be multiple address lines, multiple data lines, a clock line and various other control signals. Address or data values sent over the bus are transferred at the same time over all the parallel lines.



- One signal defined as least significant digit
- Other signals represent other digits of binary number up to most significant digit
- Manually decode bus by evaluating each signal as high (1) or low (0)
- For example, the binary value at the point highlighted above is 1001 0001. This value can also be translated as 91 hex.

To translate each group of 4 binary bits to a hex character:

Binary	Hex	Binary	Hex
0000	0	1000	8
0001	1	1001	9
0010	2	1010	A
0011	3	1011	B
0100	4	1100	C
0101	5	1101	D
0110	6	1110	E
0111	7	1111	F

ASCII Conversion Table

To translate a hex character to a ASCII character:

Hex	Char	Hex	Char	Hex	Char	Hex	Char	Hex	Char	Hex	Char
20	Space	30	0	40	@	50	P	60	`	70	p
21	!	31	1	41	A	51	Q	61	a	71	q
22	"	32	2	42	B	52	R	62	b	72	r
23	#	33	3	43	C	53	S	63	c	73	s
24	\$	34	4	44	D	54	T	64	d	74	t
25	%	35	5	45	E	55	U	65	e	75	u
26	&	36	6	46	F	56	V	66	f	76	v
27	'	37	7	47	G	57	W	67	g	77	w
28	(38	8	48	H	58	X	68	h	78	x
29)	39	9	49	I	59	Y	69	i	79	y
2A	*	3A	:	4A	J	5A	Z	6A	j	7A	z
2B	+	3B	;	4B	K	5B	[6B	k	7B	{
2C	,	3C	<	4C	L	5C	\	6C	l	7C	
2D	-	3D	=	4D	M	5D]	6D	m	7D	}
2E	.	3E	>	4E	N	5E	^	6E	n	7E	~
2F	/	3F	?	4F	O	5F	_	6F	o	7F	DEL

www.tektronix.com/serialdebug