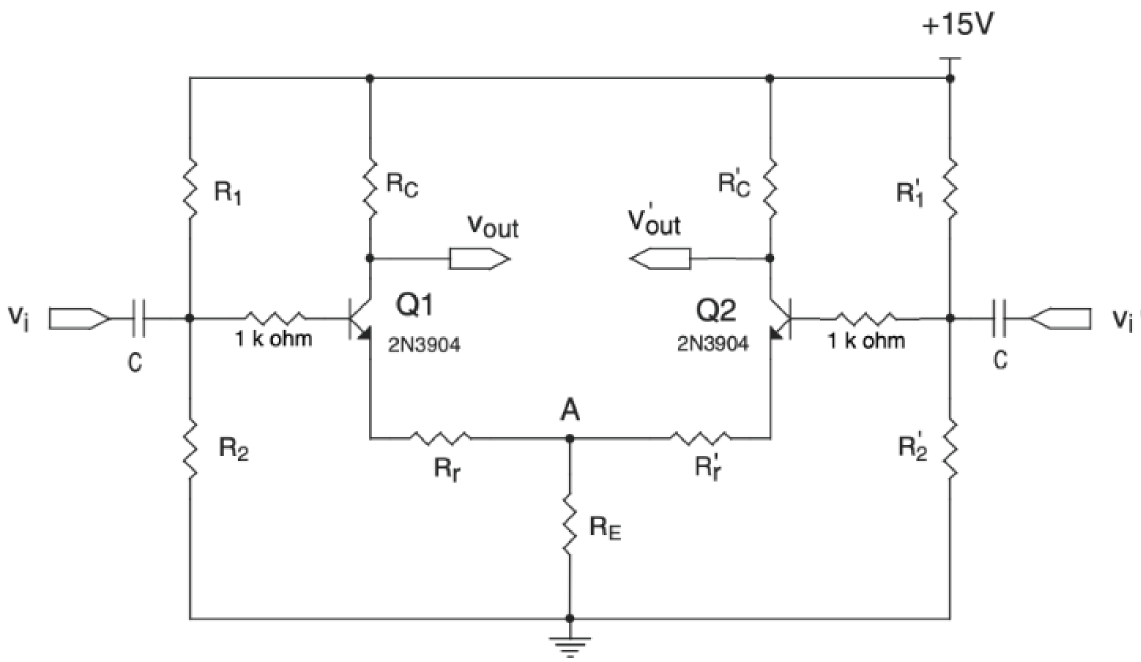
Name: ______________________________

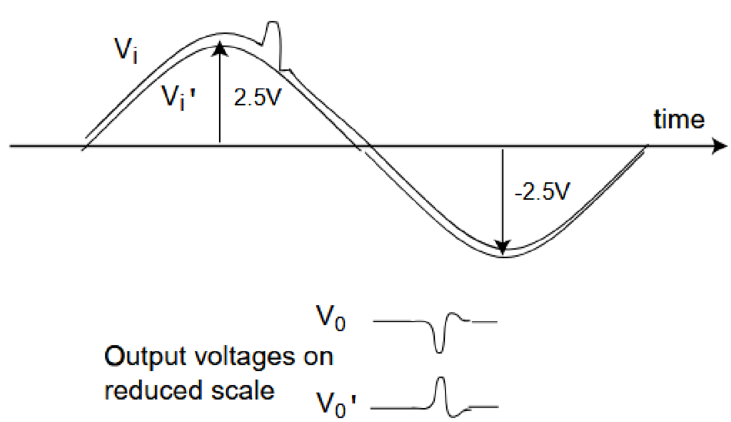
Physics 623 – Homework 3

Consider the differential amplifier below:



Set the resistor values to achieve the following design specifications, using the steps on the following pages:

- Output impedance $Z_{out} = 1\text{ k}$
- Accommodate output swings of $\pm 2\text{ V}$
- Accommodate a common-mode input range of $\pm 2.5\text{ V}$ (see plot below).
- Difference mode gain $A_d \approx 8$.



Start b assuming large β. The circuit components will be symmetrical (e.g. $R_C = R'_C$), but the inputs may not be.

a) Our transistor model assumes large resistance (~ 1 MΩ) looking into the collector, and therefore $Z_{out} = R_C$. This sets the value of R_C.

$R_C =$ ____________________

b) As we'll see in part (e), we would like to have the Quiescent collector currents I_C as small as possible while still avoiding cutoff. What is the smallest Q-point I_C which would ensure $I_C \geq 0$ even for ± 2 V output swings? (*Hint:* It may help to think in terms of voltages. For small I_C, V_C is not much less than 15 V. But we need to accommodate a $\pm$2V, so it needs to be at least 2V less, i.e. we want $V_C = 13\text{V}$.)

$I_C =$ ____________________

c) Calculate the necessary value of R_r to achieve the desired differential-mode gain. Include the effects of transresistance $r_{tr} = 0.025\text{V}/I + 2\Omega$, where I is the current through the emitter of the transistor (assuming large beta, you have already calculated this current).

$R_r =$ ____________________

d) What is the quiescent current through R_E?

$I_E =$ ____________________

e) Calculate the optimal value for R_E. First, recall the formulas for the common-mode gain A_C and the Common Mode Rejection Ratio CMRR. To minimize A_C and maximize CMRR, R_E should be maximized. This means a relatively large $V_A \approx V_E$.

To avoid saturation, we need to ensure $V_C - V_E \gtrsim 0.5\text{V}$ and remains so during input or output swings. The worst-case scenario would be a negative output swing (brining V_C down) coupled with a positive common-mode input swing (bringing V_E up). The following calculations should be easily done in your head:

a. Based on previous answers, what would be the collector voltage in this worst-case scenario?

b. What then is the upper limit on V_E in this scenario?

c. Since we are assuming a worst-case +2.5V input swing, what would be the value of V_E at the Q-point?

Now use your value for I_E to compute R_E.

$R_E =$ ______________________

f) Finally, we set our bias resistors R_1 and R_2. We have two constraints on these two unknowns:

1. In the limit of large beta, we can determine the Q-point V_B, which is related to the power supply +15 V.
2. In the limit $\beta \to \beta_{min}$, we need to ensure our Q-point doesn't move too much. Take $\beta_{\text{min}} = 75$, and say we want the base voltage to differ from its large-β value by no more than 0.2 V. In other words, we need the voltage drop across the Thevenin-equivalent bias network with $I_B = I_C/\beta_{\text{min}}$ to be at most 0.2 V.

Use these constraints to set R_1 and R_2.

$R_1 =$ ______________________

$R_2 =$ ______________________